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REVISION : 07242-1

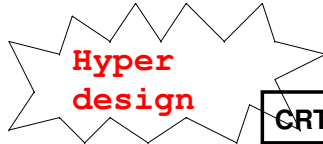



Diagram illustrating the layer structure of a 4-layer PCB. The layers are labeled from top to bottom: TOP, GND, S, S, PWR, S, GND, and BOTTOM. The GND and PWR layers are shown as thicker lines, indicating they are ground and power planes, respectively. The S layers are thinner lines representing signal layers.

BOM			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLOCK DIAGRAM			
Size A3	Document Number	LT32P	Rev -1
Date:	Wednesday, June 18, 2008	Sheet	1 of 53

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC2(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC2(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLEPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0] [P, N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

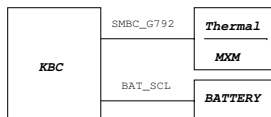
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

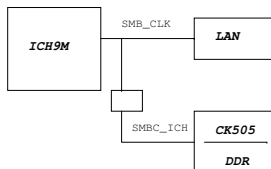
17,43,44,46,47,48,49,50,51	DCBATOUT	DCBATOUT
7,28,38,43,51,53	3D3V_AUX_S5	3D3V_AUX_S5
40,43,51	5V_AUX_S5	5V_AUX_S5
13,25,26,27,29,30,35,37,38,39,41,42,43,48,49,50,51,53	3D3V_S5	3D3V_S5
17,28,31,42,43,46,47,48,49,50	5V_S5	5V_S5
10,12,13,15,16,29,39,48,50	1D5V_S3	1D5V_S3
15,16,48	0D75V_S3	0D75V_S3
17,49,50	1D8V_S3	1D8V_S3
3,7,10,11,13,15,16,17,18,23,24,25,26,27,28,29,30,31,32,33,34,35,38,39,40,41,44,46,50,51,53	3D3V_S0	3D3V_S0
7,13,18,21,24,25,29,30,31,34,42,44,50,51,53	5V_S0	5V_S0
4,5,6,8,10,11,12,13,28,29,44,46	1D05V_S0	1D05V_S0
3,5,13,26,28,29,34,40,41,50,53	1D5V_S0	1D5V_S0
19,21,22,23,24,50	1D8V_S0	1D8V_S0
20,21,23,48	1D1V_S0	1D1V_S0
21,23,24,47	VGA_CORE_S0	VGA_CORE_S0

SMBus



USB Table

Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1



PCI Routing

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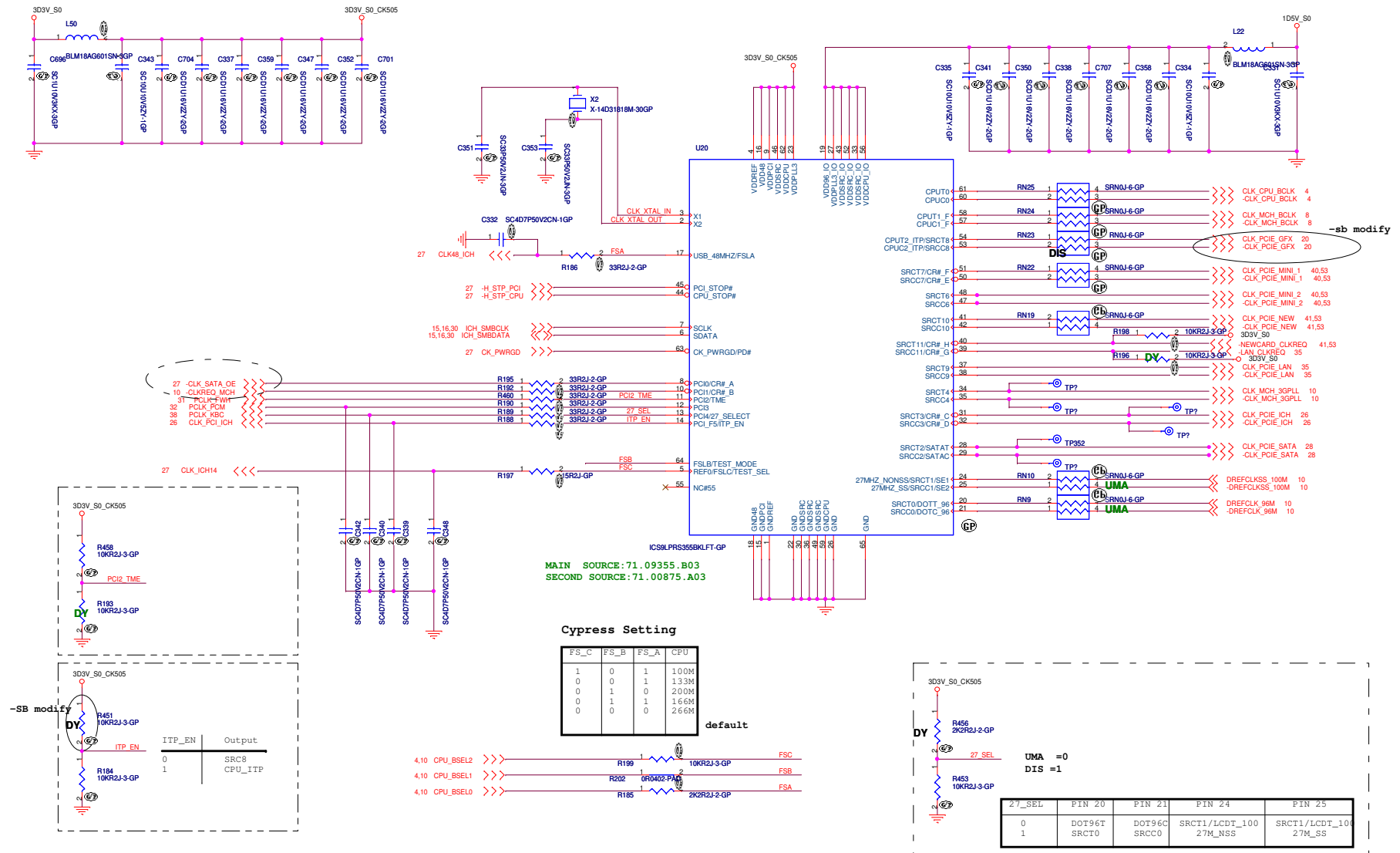
IT17412	IDSEL	INT	REQ	GNT
	AD22	G:CARBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

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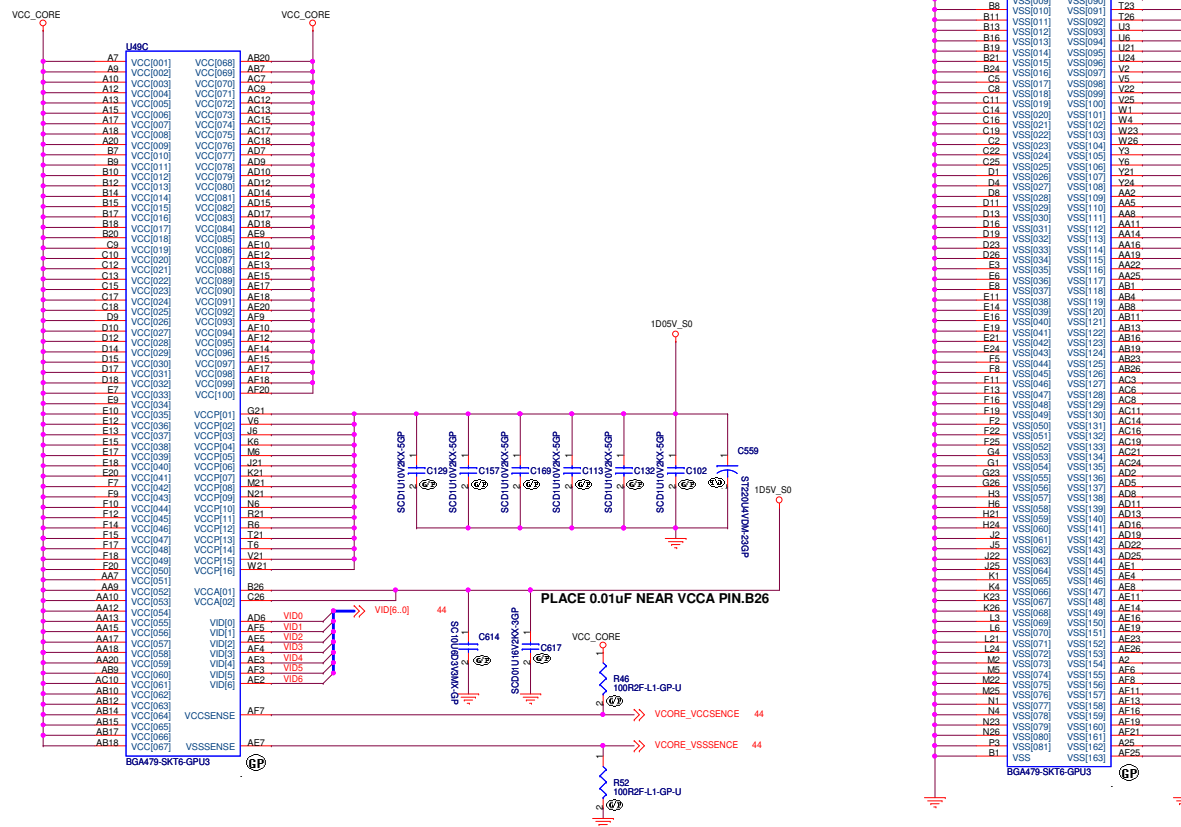
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Title	Reference
Size	Document Number
Date: Wednesday, July 09, 2008	Olympus
Sheet 2	Rev -1



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

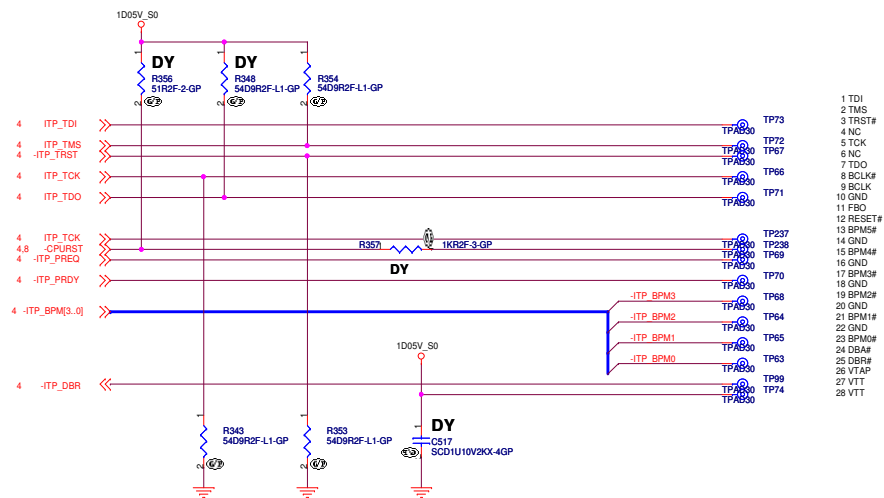
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Title			
Penryn CPU(2/2)			
Size	Document Number		Rev
C		Olympus	-1
Date:	Wednesday, July 09, 2006	Sheet 5 of	53



(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

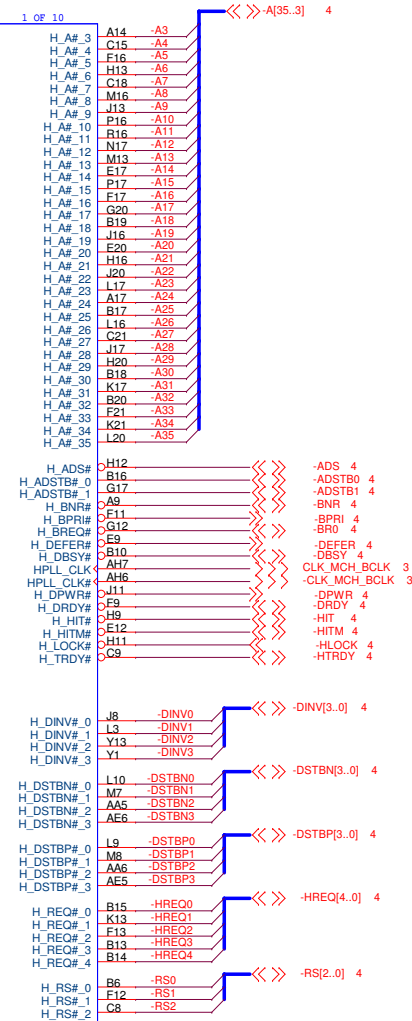


Title			
Thermal/Fan Controller G792			
Size	Document Number	Rev	
C	Olympus	-1	
Date:	Wednesday, July 09, 2008	Sheet 7 of	53

Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

HOST



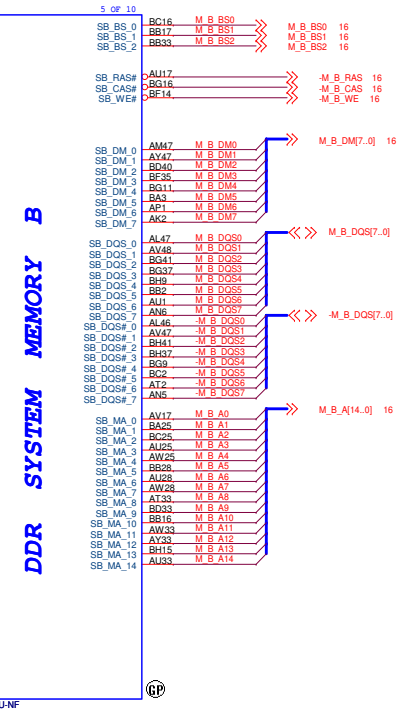
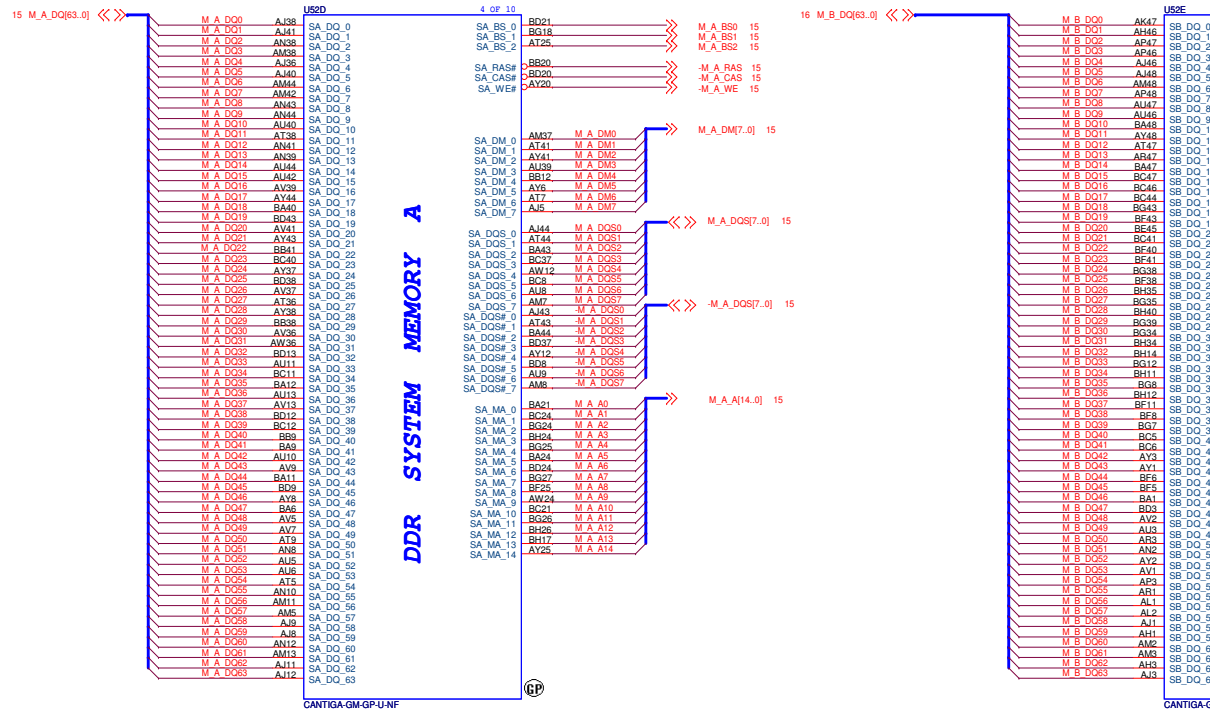
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Title
Cantiga(1/7):HOST I/F

Size A3 Document Number
Olympus

Date: Wednesday, June 18, 2008 Sheet 8 of 53



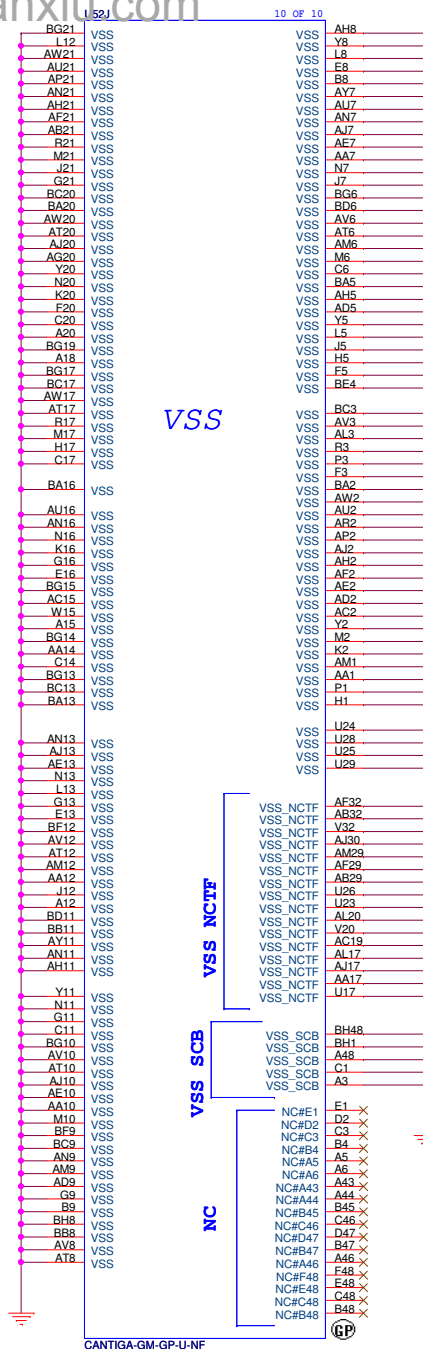
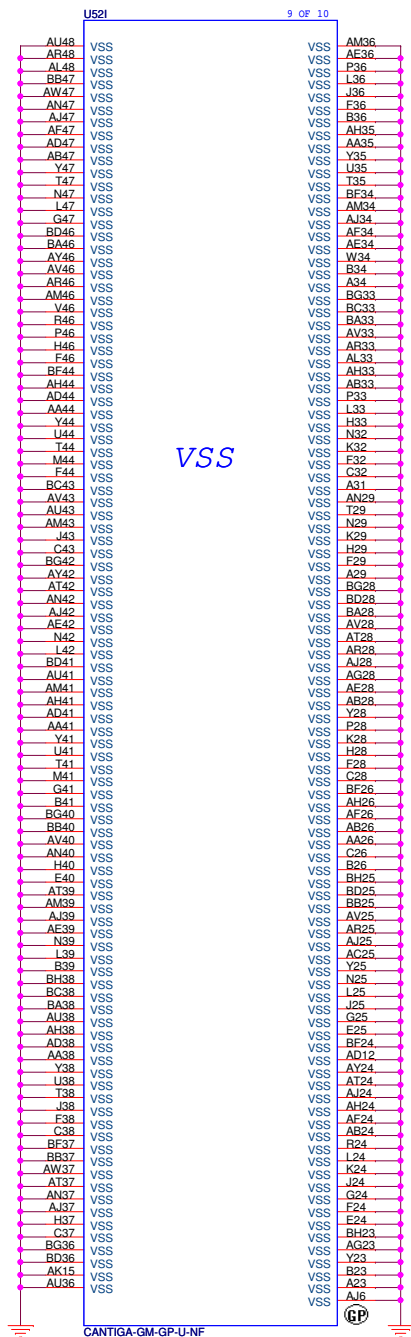
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File	Cantiga(27):DDR3		
Size	Document Number	Rev	-1
C	Olympus		
Date: Wednesday, June 18, 2008	Sheet 9	of	53

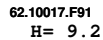
CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown



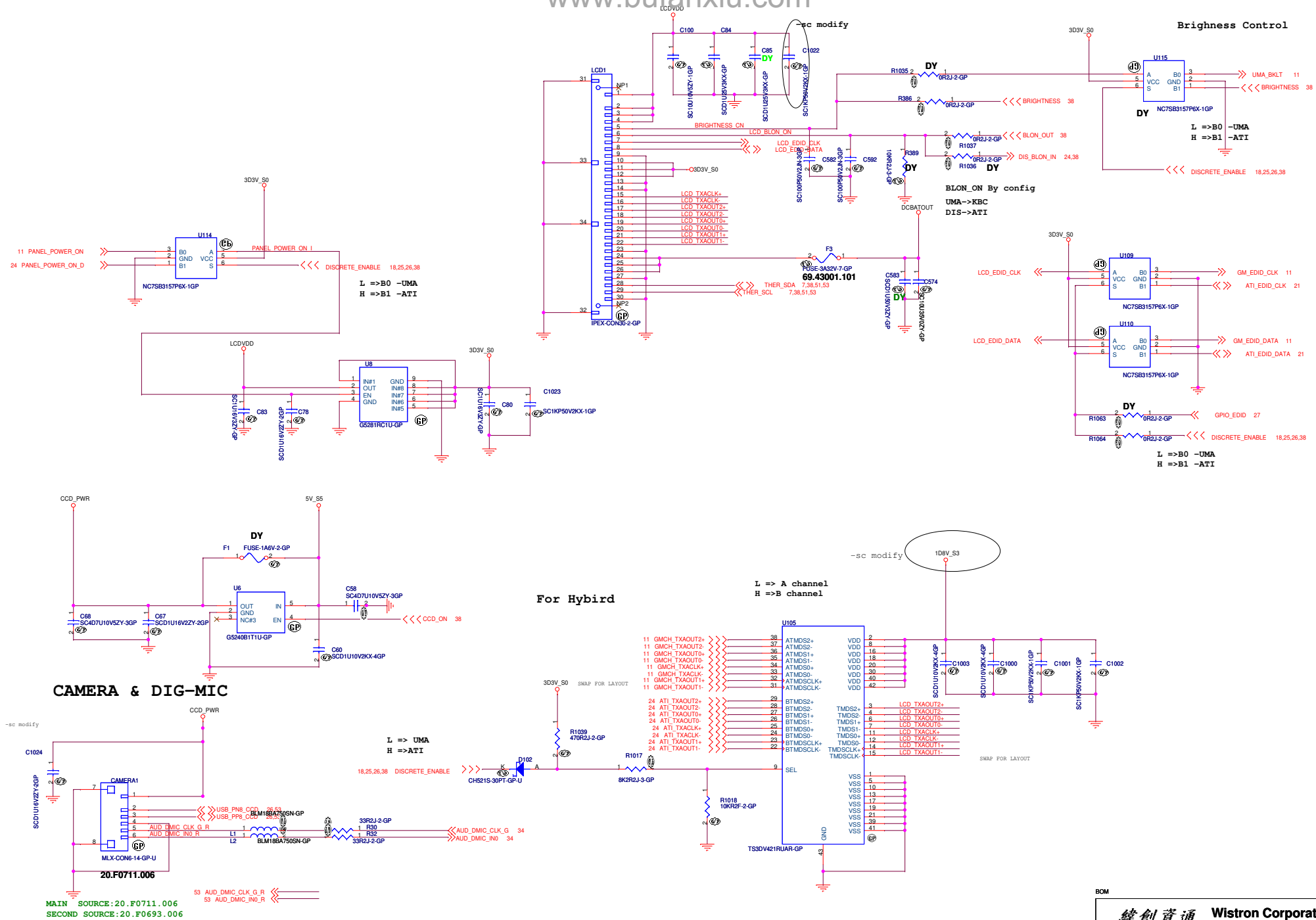


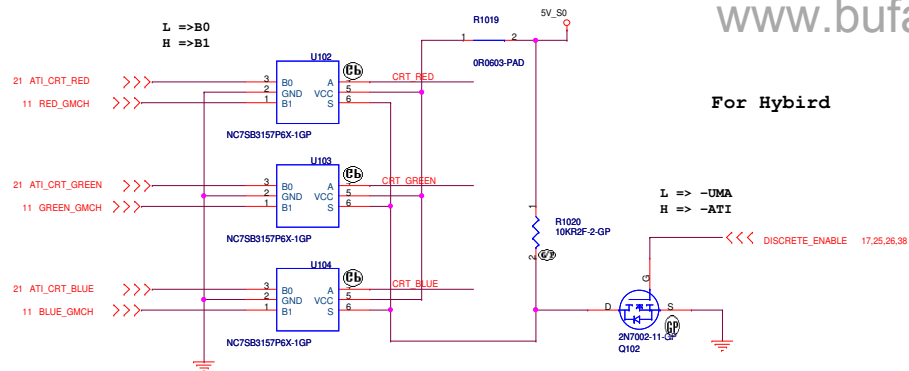
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Size	Document Number
A3	
Olympus	
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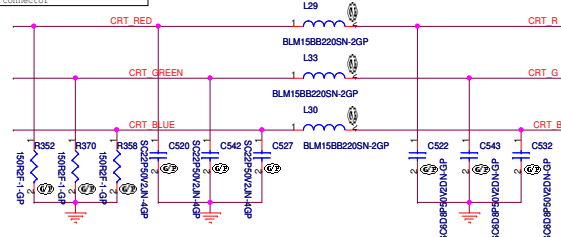
Title DDR3 SODIMM-A (NORMAL TYPE)			
Size C	Document Number Olympus		Rev -1
Date: Wednesday, July 09, 2008	Sheet 15	of	53





Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

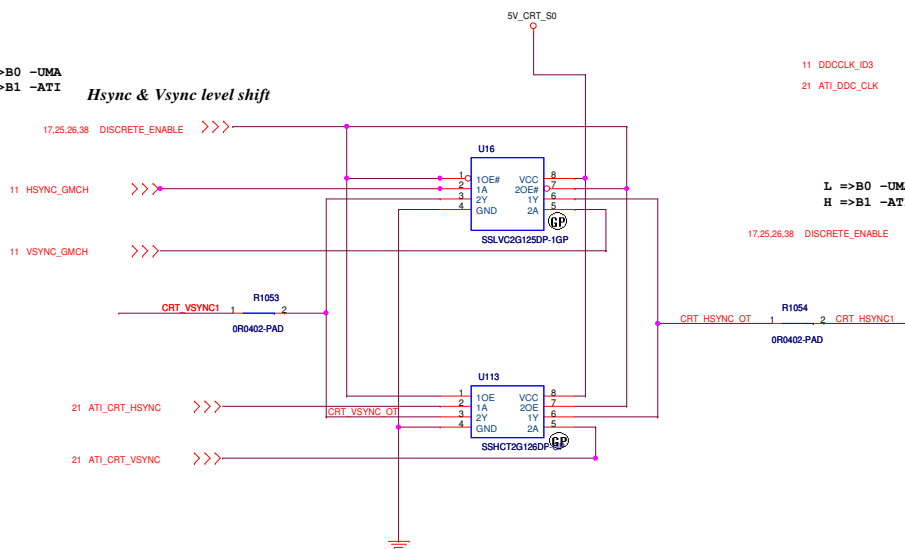


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

L ==> B0 -UMA
H ==> B1 -ATI

Hsync & Vsync level shift



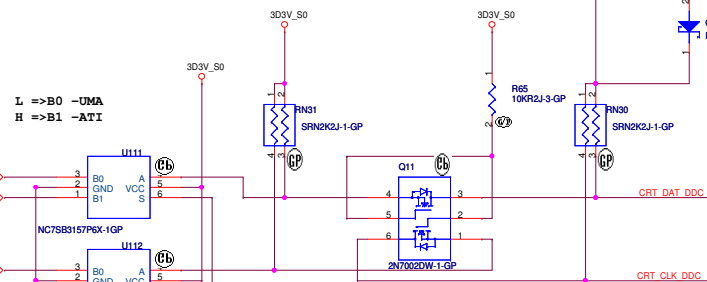
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H ==> B1 -ATI

11 DDCDATA_ID1 >>>
21 ATI_DDC_DATA >>>

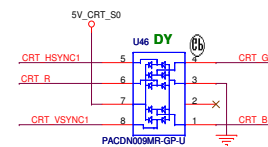
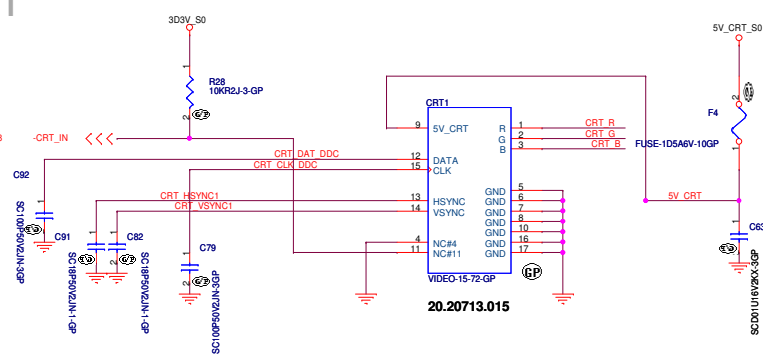
11 DDCCLK_ID3 >>>
21 ATI_DDC_CLK >>>

L ==> B0 -UMA
H ==> B1 -ATI

17,25,26,38 DISCRETE_ENABLE >>>



DDC_CLK & DATA level shift



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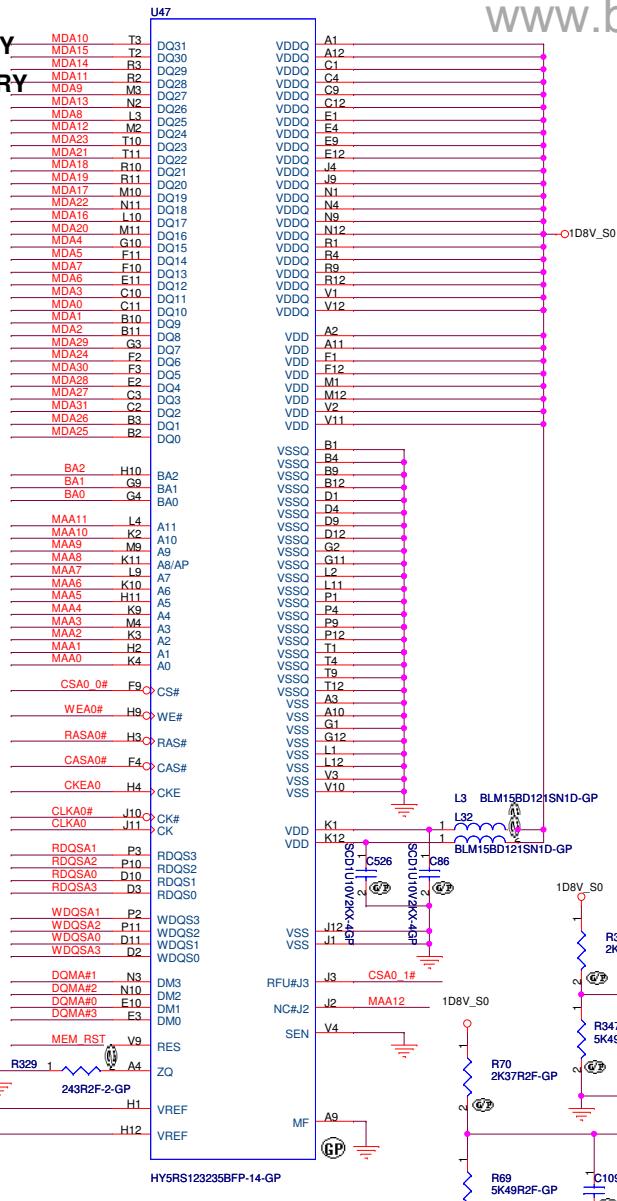
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Size	Document Number	Rev	-1
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LAB1 GDDR3 16MX32 MEMORY

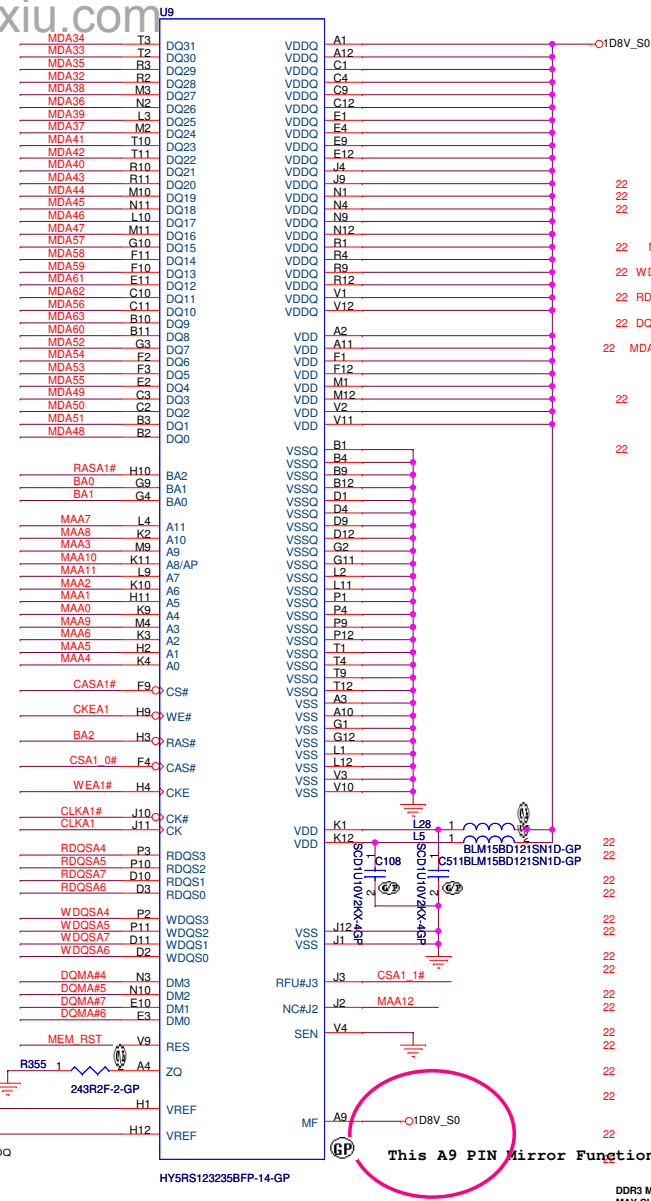
LAB2 GDDR3 32MX32 MEMORY

72.41032.B0U SAMSUNG

72.18512.I0U QIMONDA



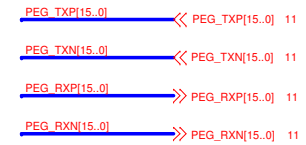
PLACE VREF DIVIDER COMPONENTS
AS CLOSE TO MEMORY AS POSSIBLE



DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M625, M645, M715 AND M725.
SEE DATA BOOK FOR LATEST INFORMATION

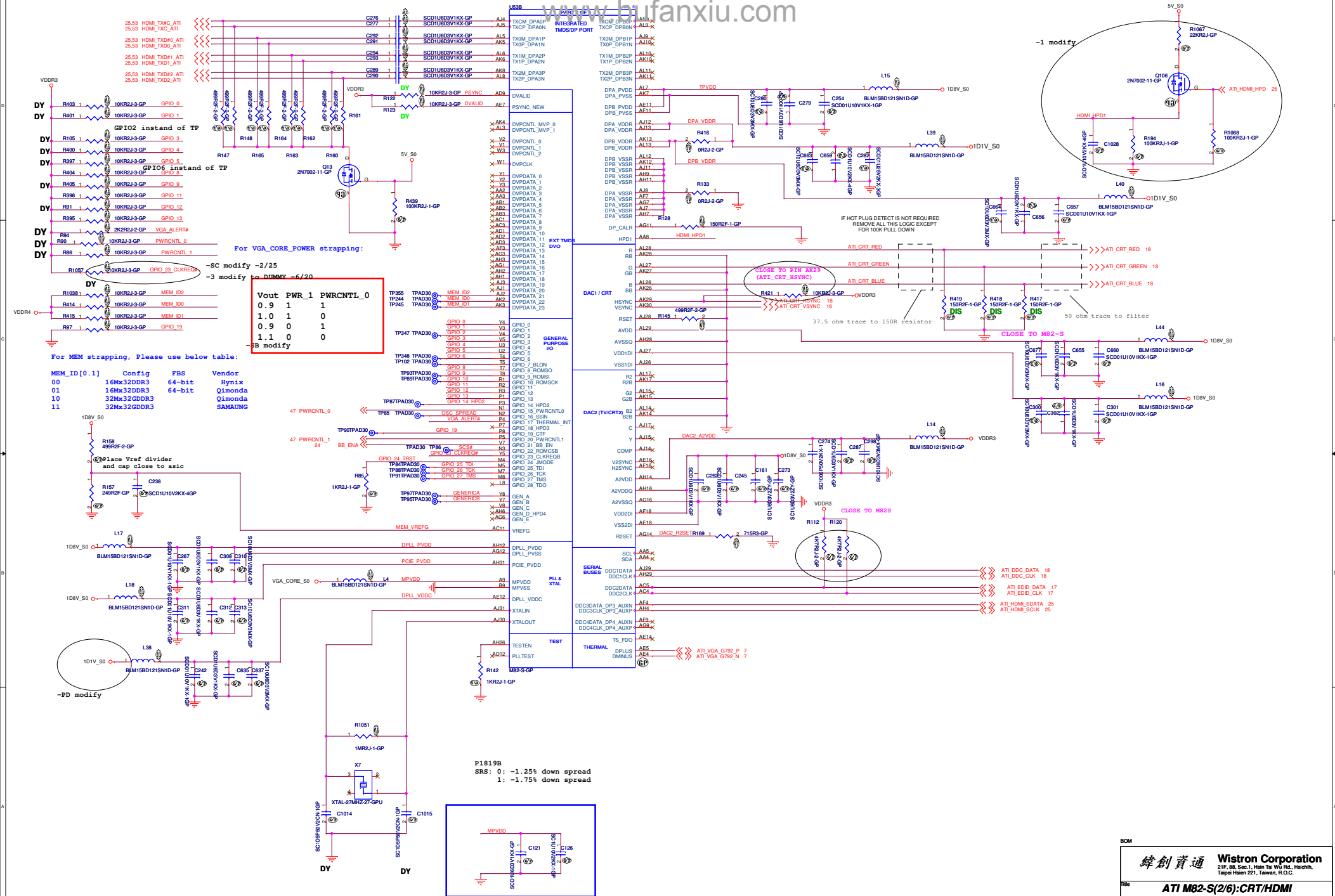
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Size A3	Document Number	Olympus	Rev -1
Date: Wednesday, July 09, 2008	Sheet 19	of	53



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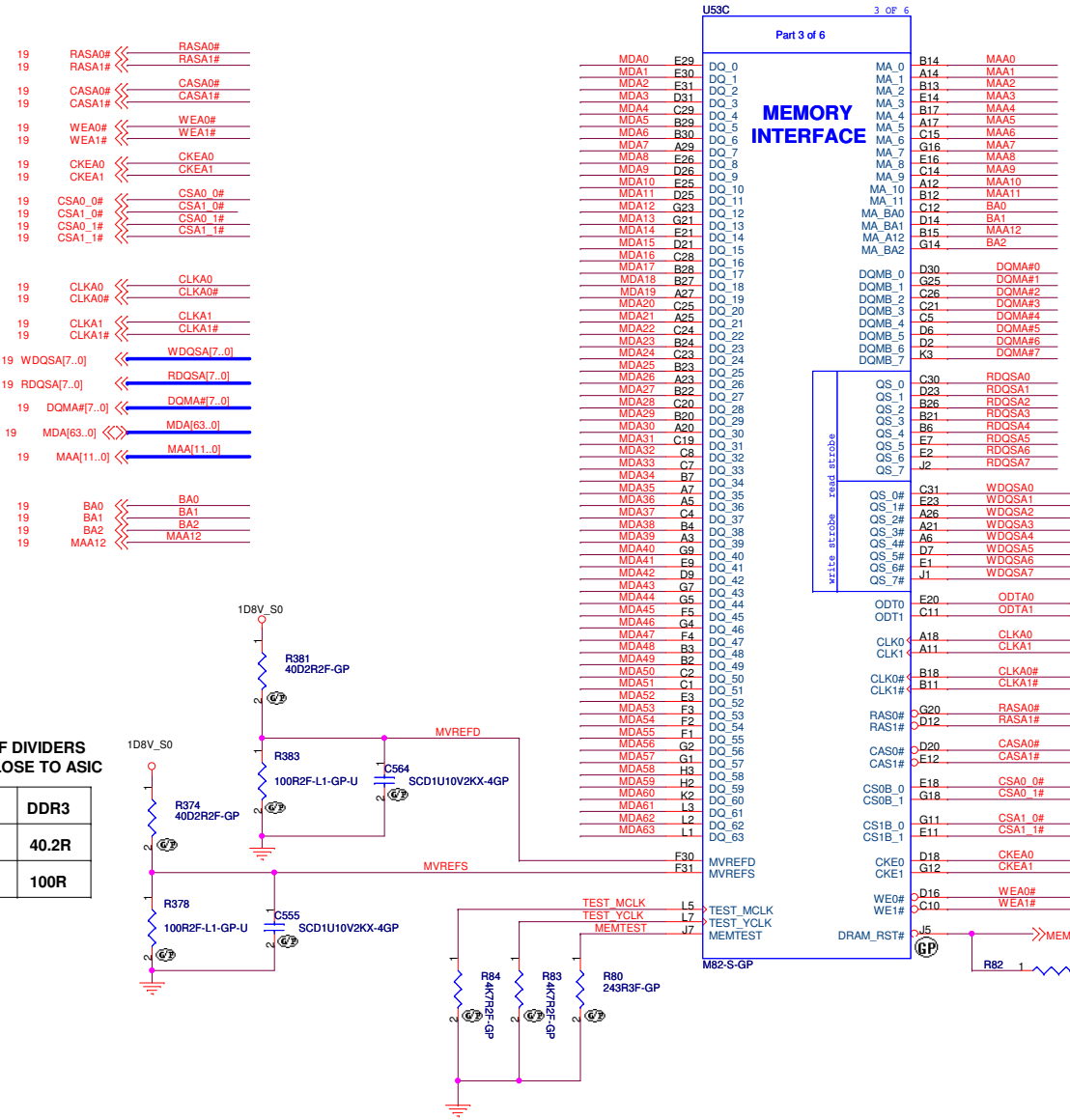
Sheet 20 of 53



Pls place these capacitors as close to as U14 MPVDD Pin.

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



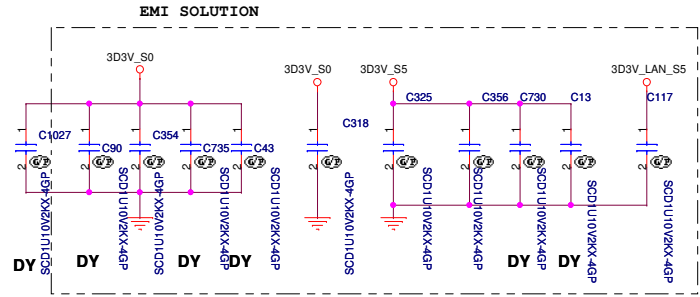
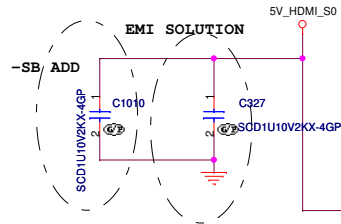
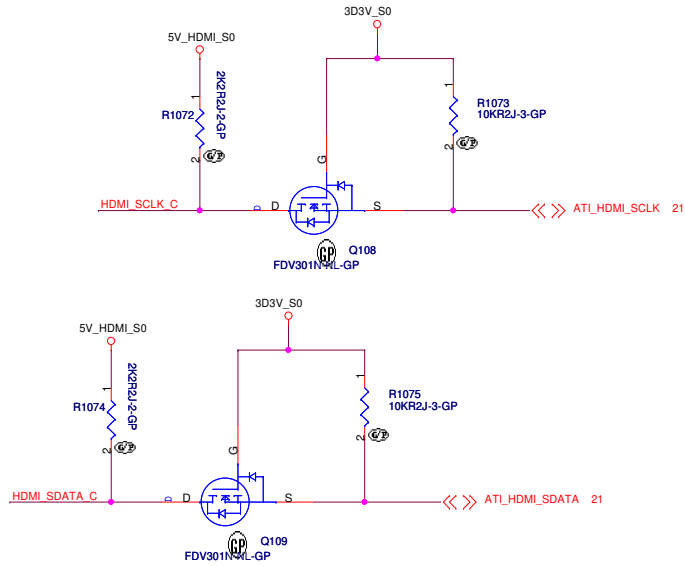
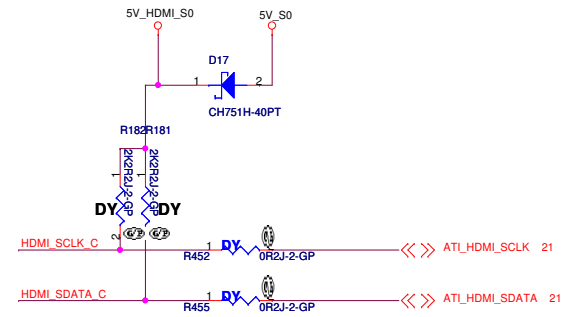
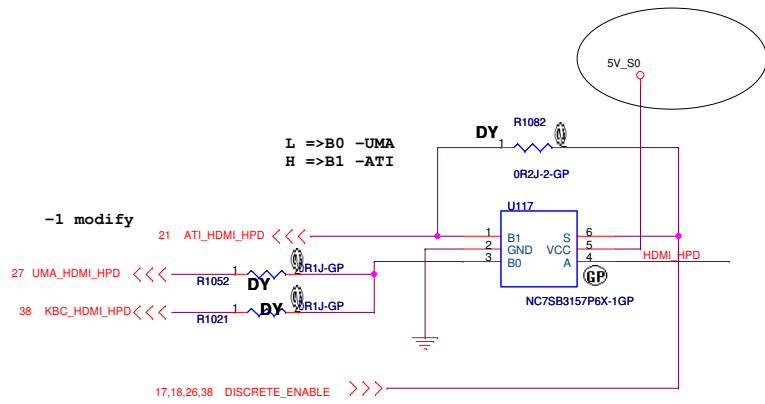
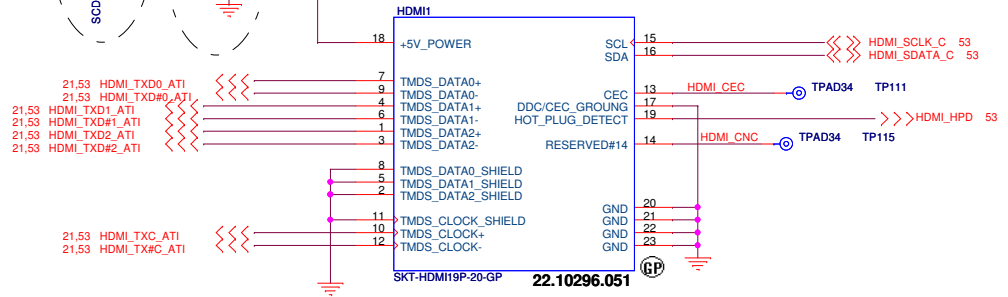
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Size A3	Document Number Olympus
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Title			
ATI M82-S(6/6):LVDS			
Size	Document Number		Rev
Custom	Olympus		-1
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**HDMI CONN**

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Title

HDMI CONN

Size
A2

	Document Number
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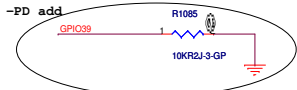
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Rev
-1

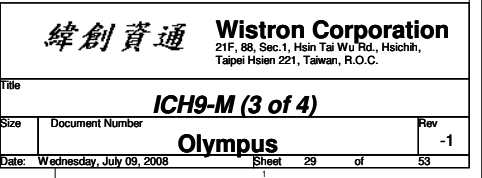


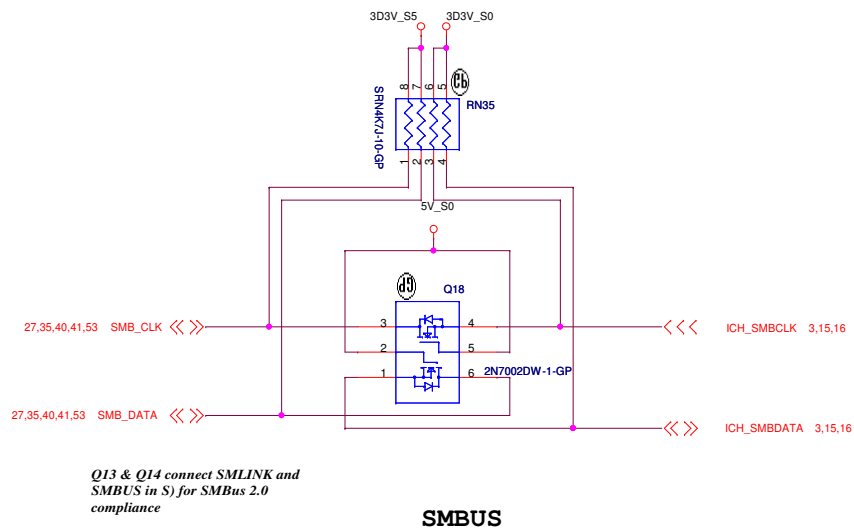
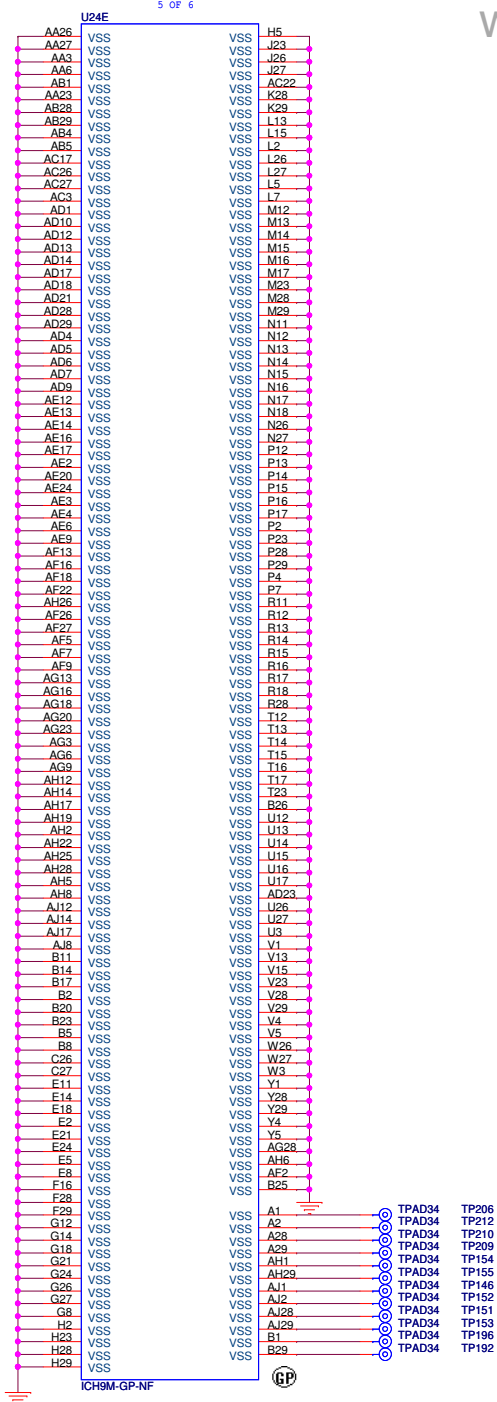




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Size	Document Number		Rev
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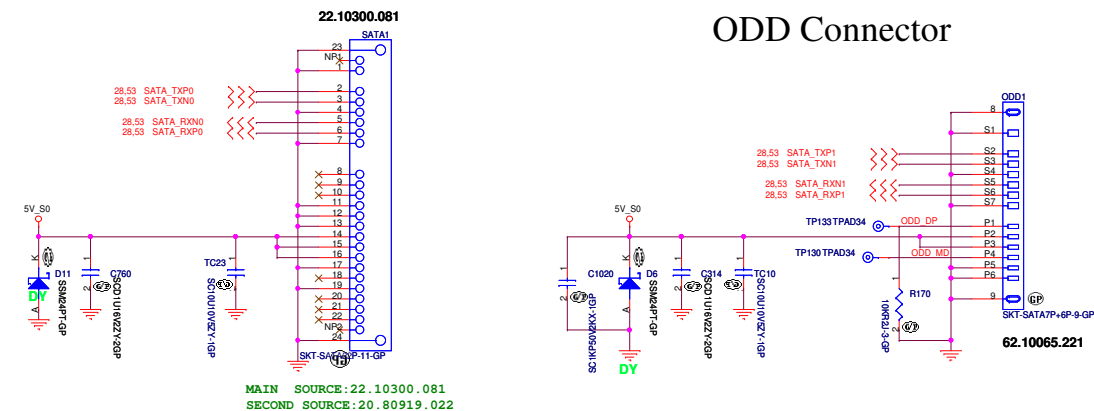




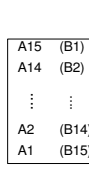
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Size	Document Number		Rev -1
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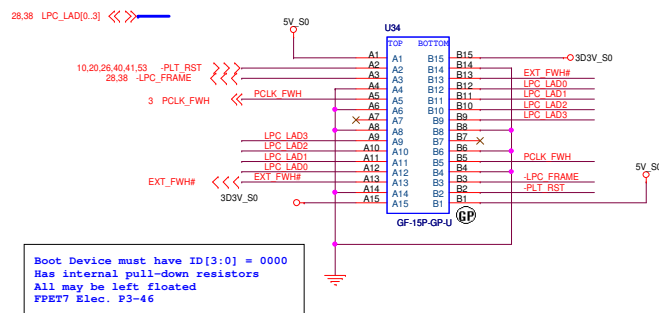
ODD Connector



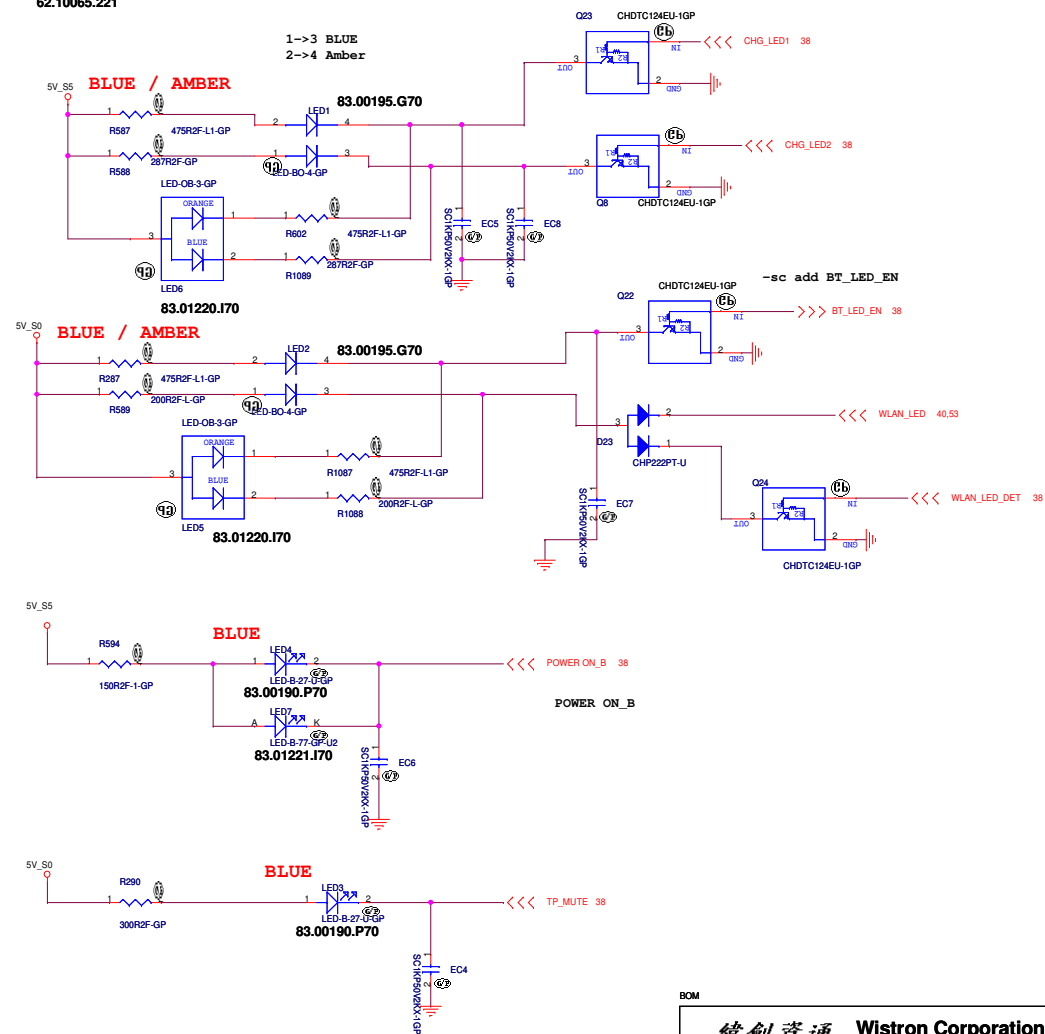
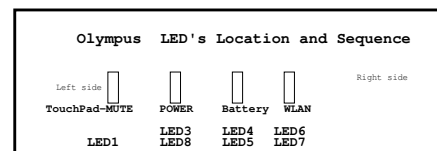
TOP VIEW



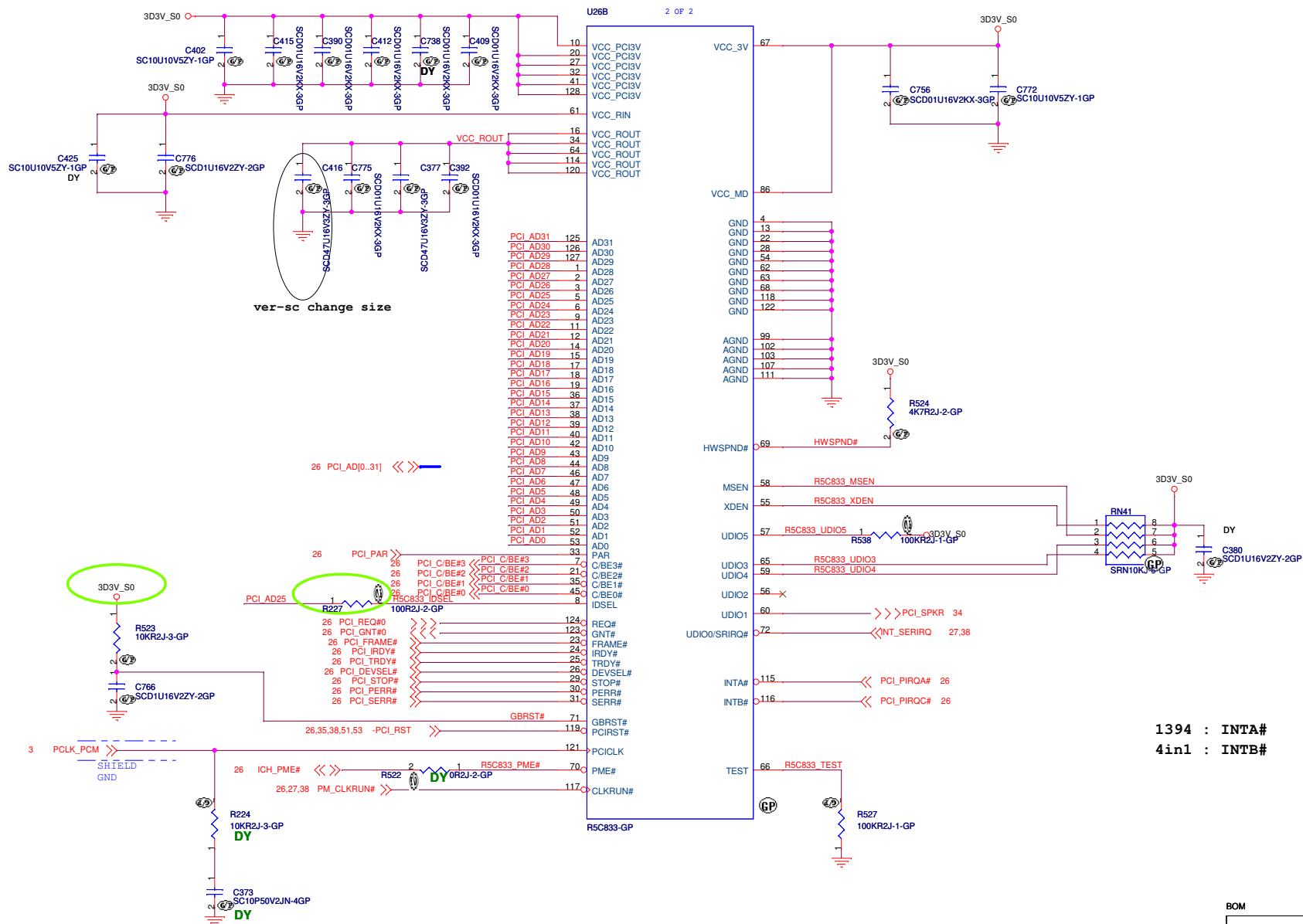
GOLDEN FINGER FOR DEBUG BOARD



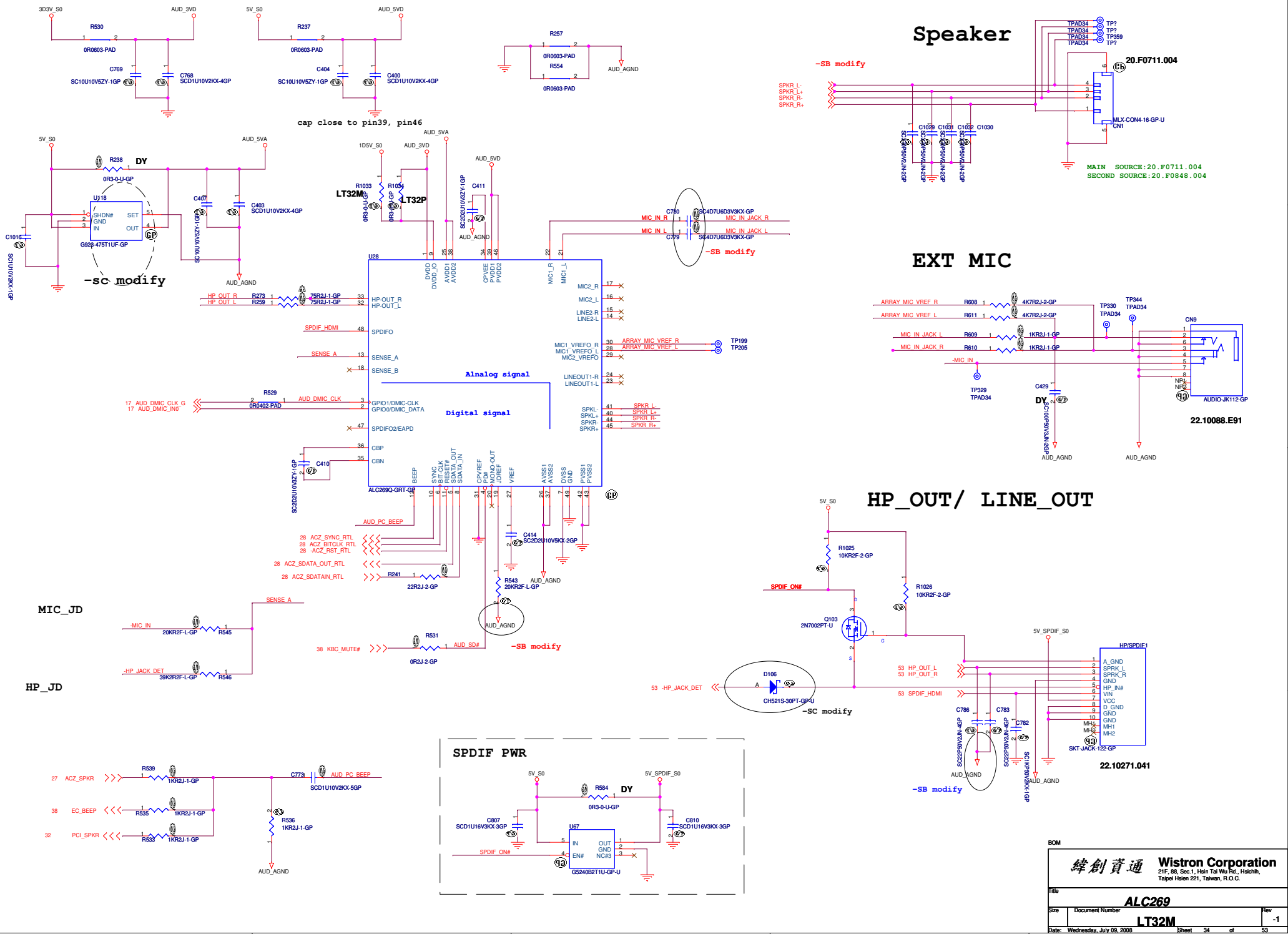
(BOTTOM VIEW)

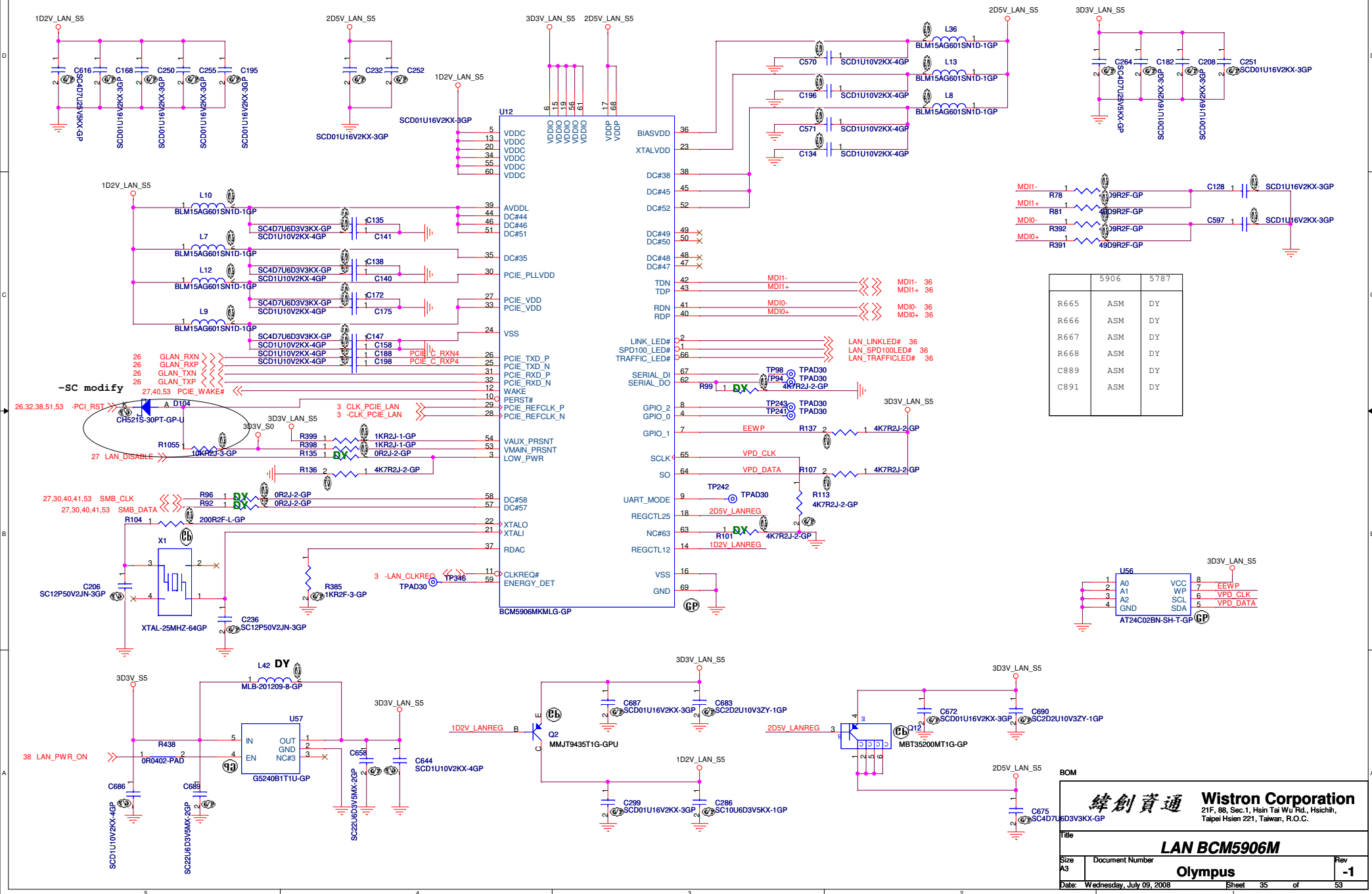


BOM

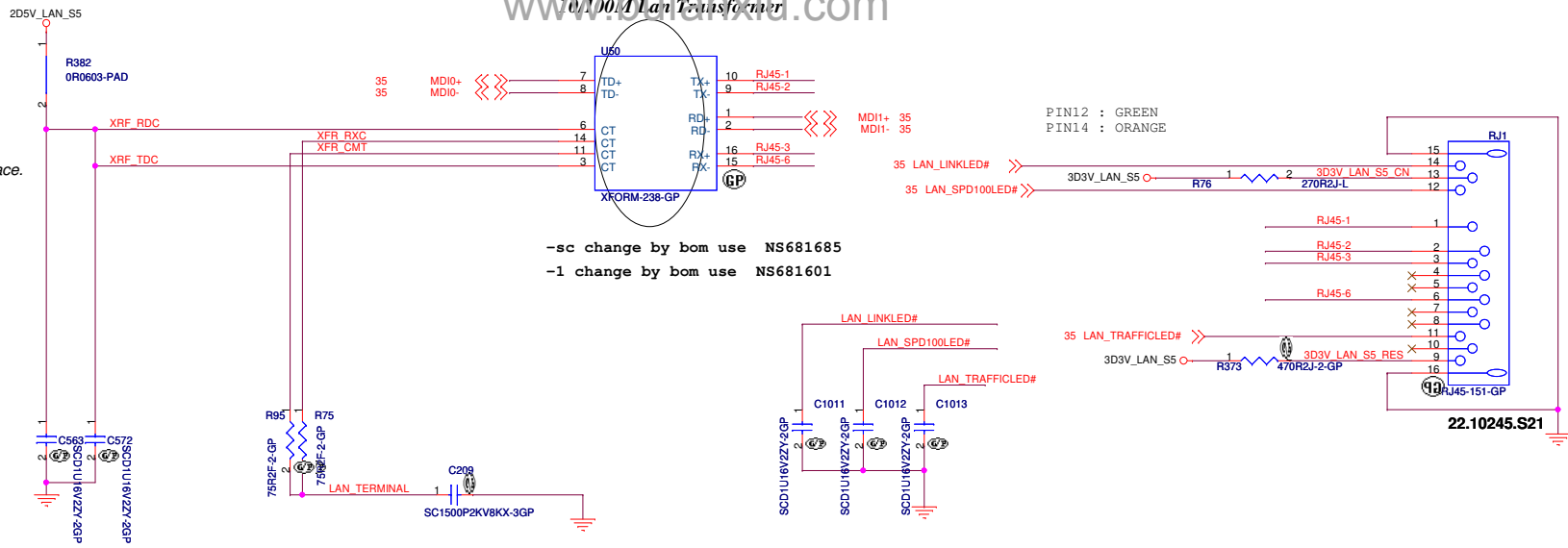


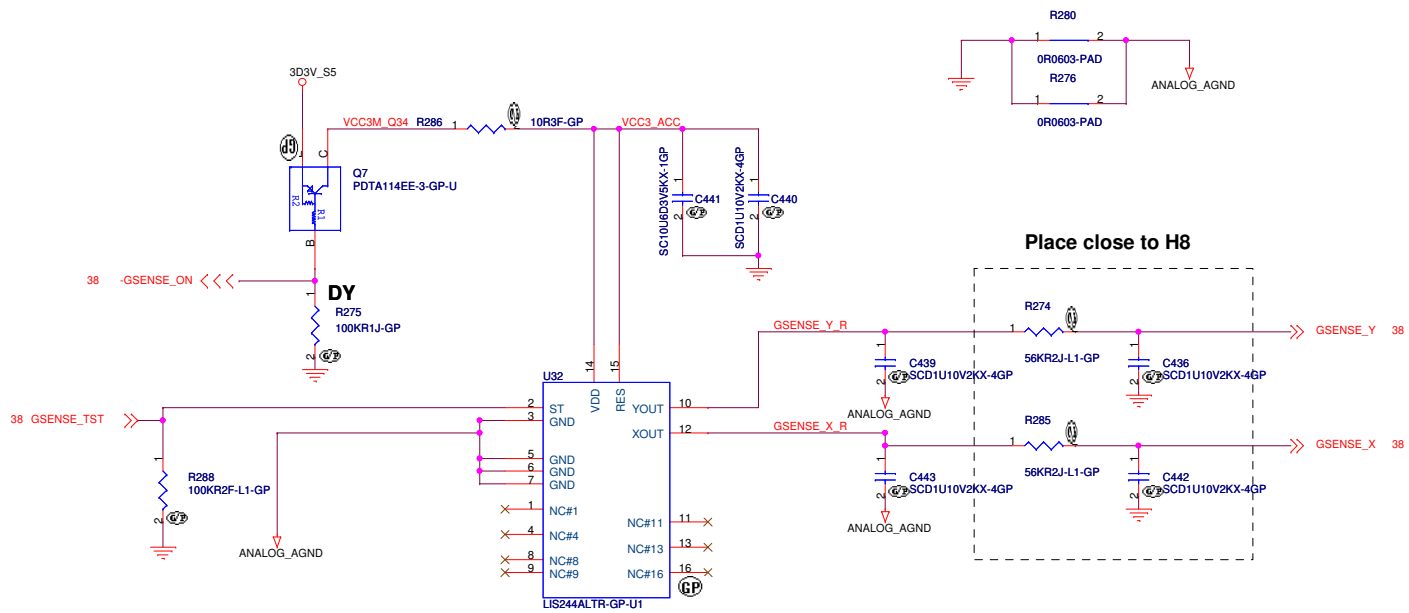
```
1394 : INTA#
4in1  : INTB#
```



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.





Primary : STMicro LIS244AL
2nd: ADI ADXL322

**Width = 6 mil & Spacing = 10 mil
for three Output traces**

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

[illegible]

G-SENSOR

Size
A3

Document Number

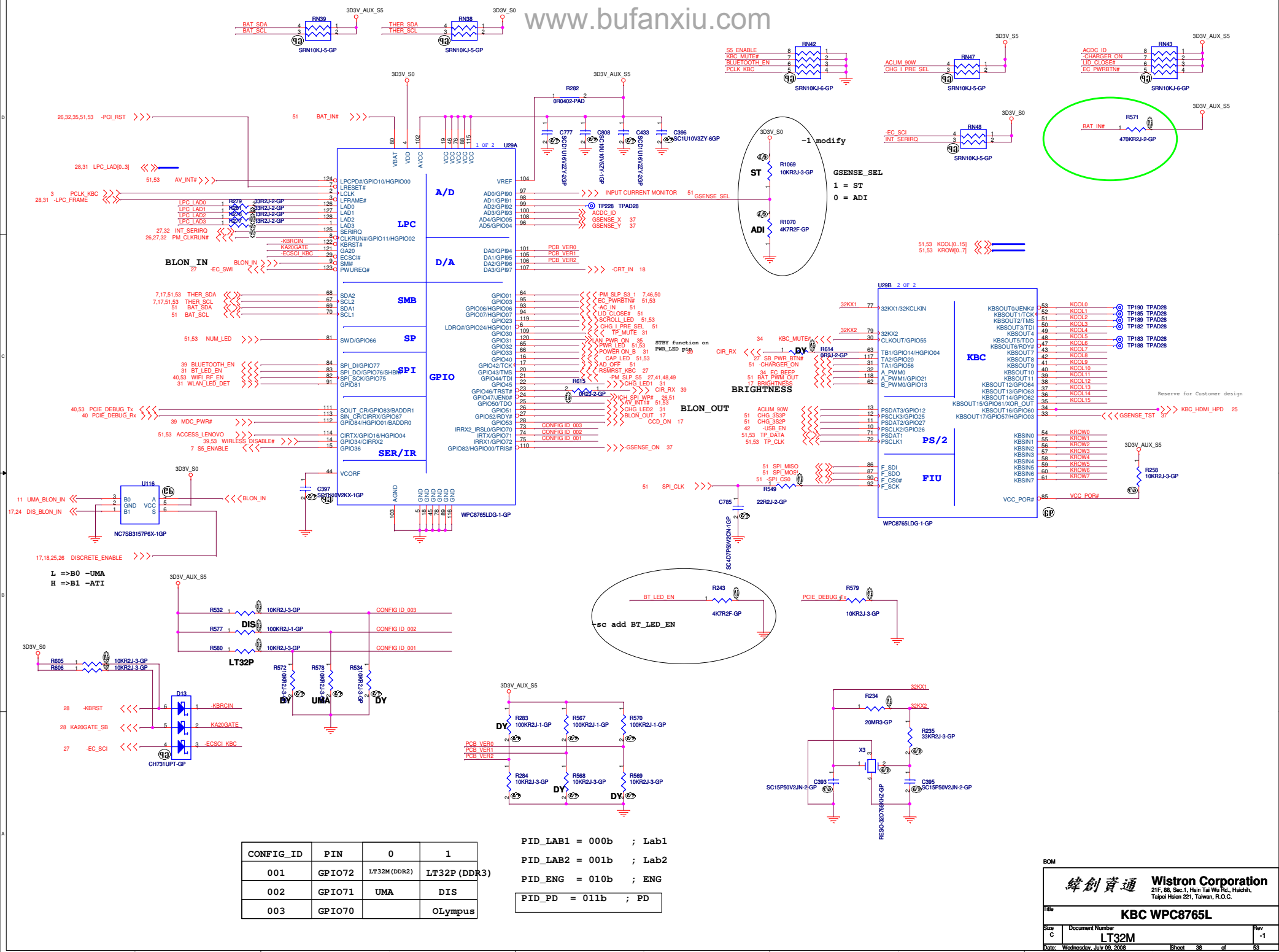
Olympus

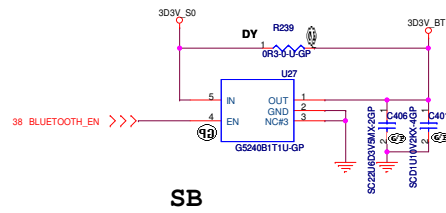
Rev
-1

Date: Wednesday, June 18, 2008

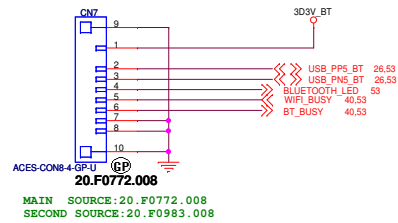
Sheet

E

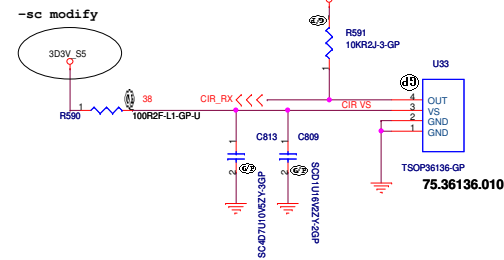




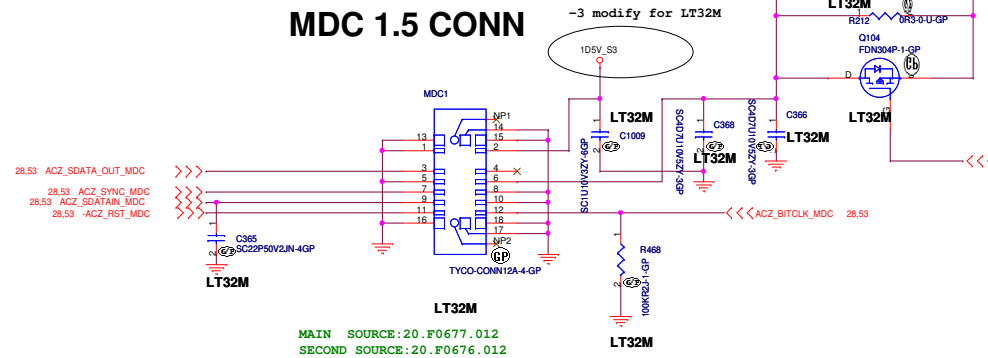
BT CONNECTOR



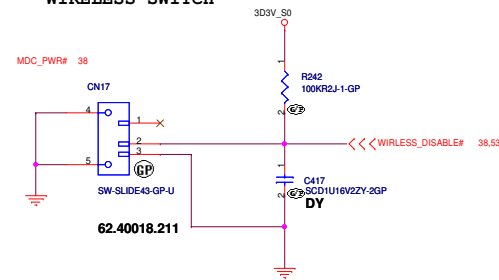
CIR



MDC 1.5 CONN



WIRELESS SWITCH



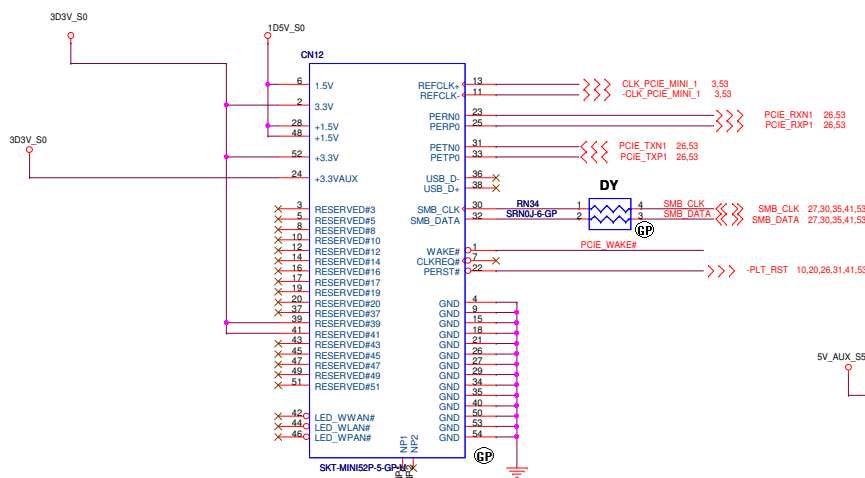
BOM

Mini PCI-E Connector

Only port-1 support USB

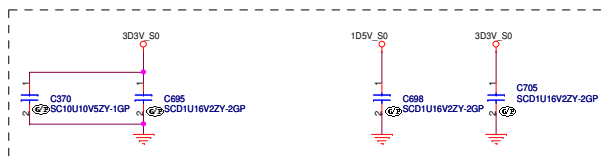
For Robson

Port-1 High



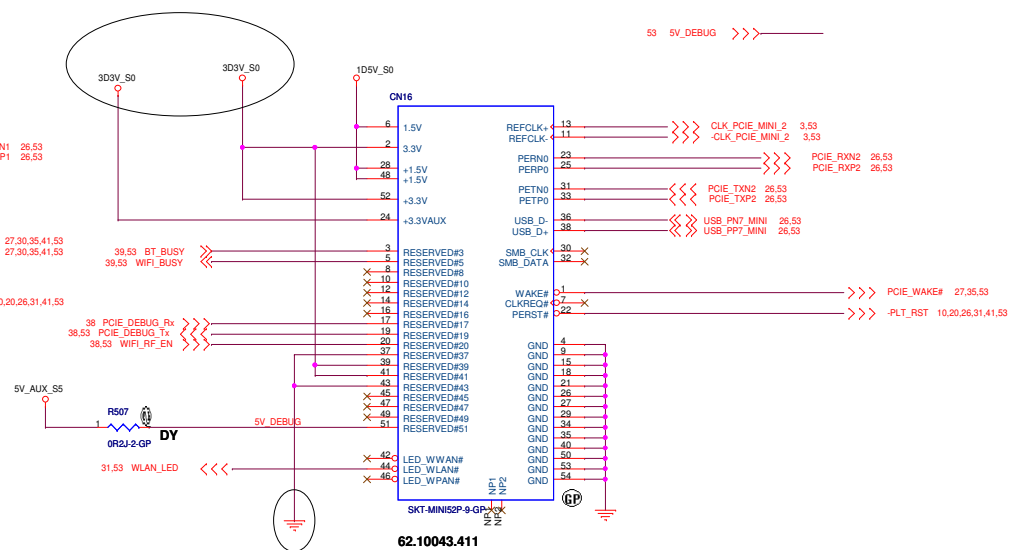
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SECOND SOURCE:20.F1107.052



Mini PCI-E Connector

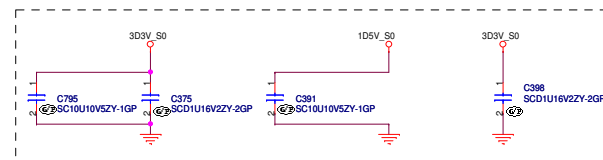
Port-2 low



62.10043.411

MAIN SOURCE:62.10043.411

SECOND SOURCE:20.F1084.052



BOM

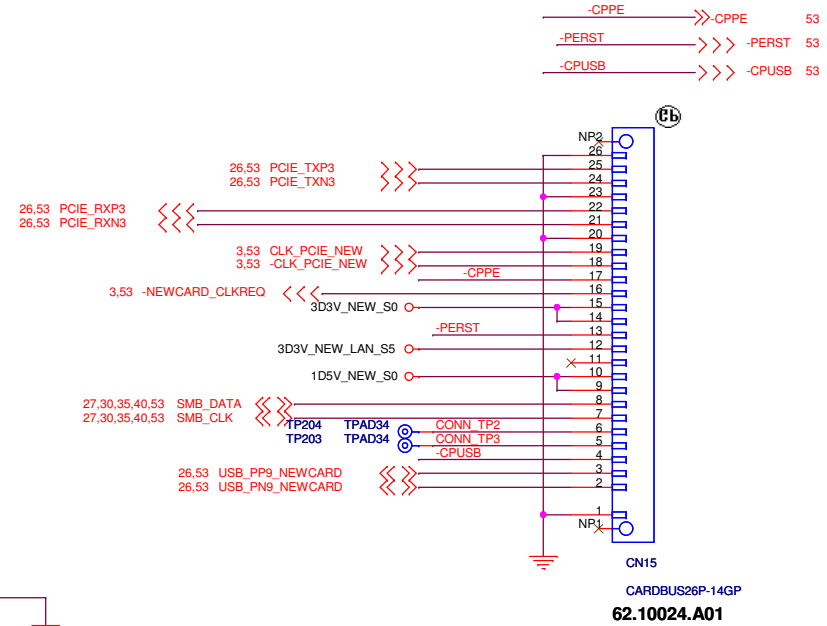
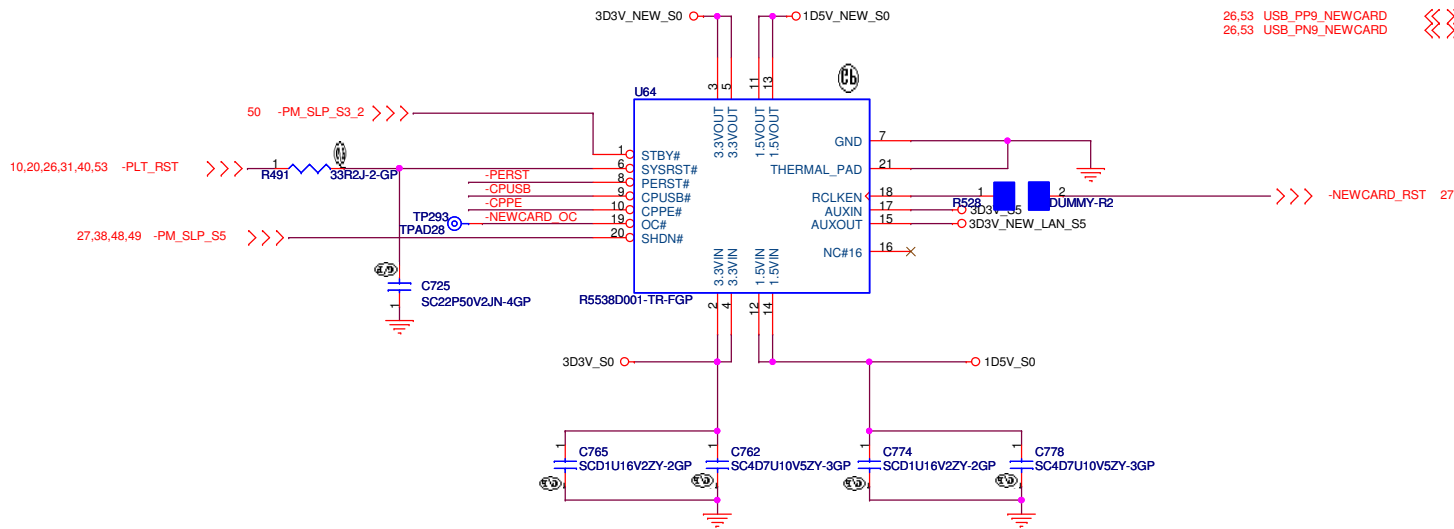
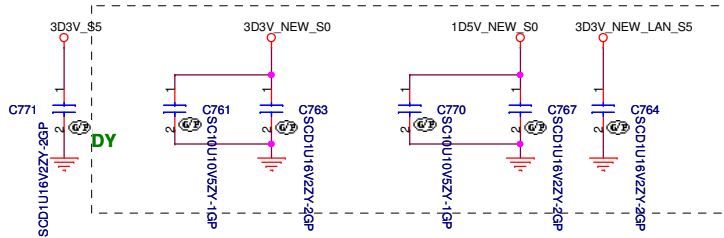
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

File MINI CARD CONN.
Size Document Number Rev
C Olympus -1
Date: Wednesday, July 09, 2008 Sheet 40 of 53

NEWCARD Connector

Place them Near to Chip

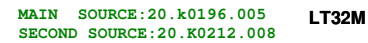
Place them Near to Connector



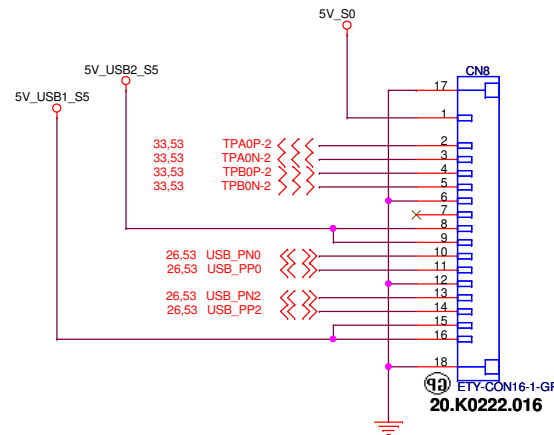
BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Module NewCard			
Size	Document Number	Rev	-1
Date: Wednesday, July 09, 2008	Sheet	41	of 53

1394

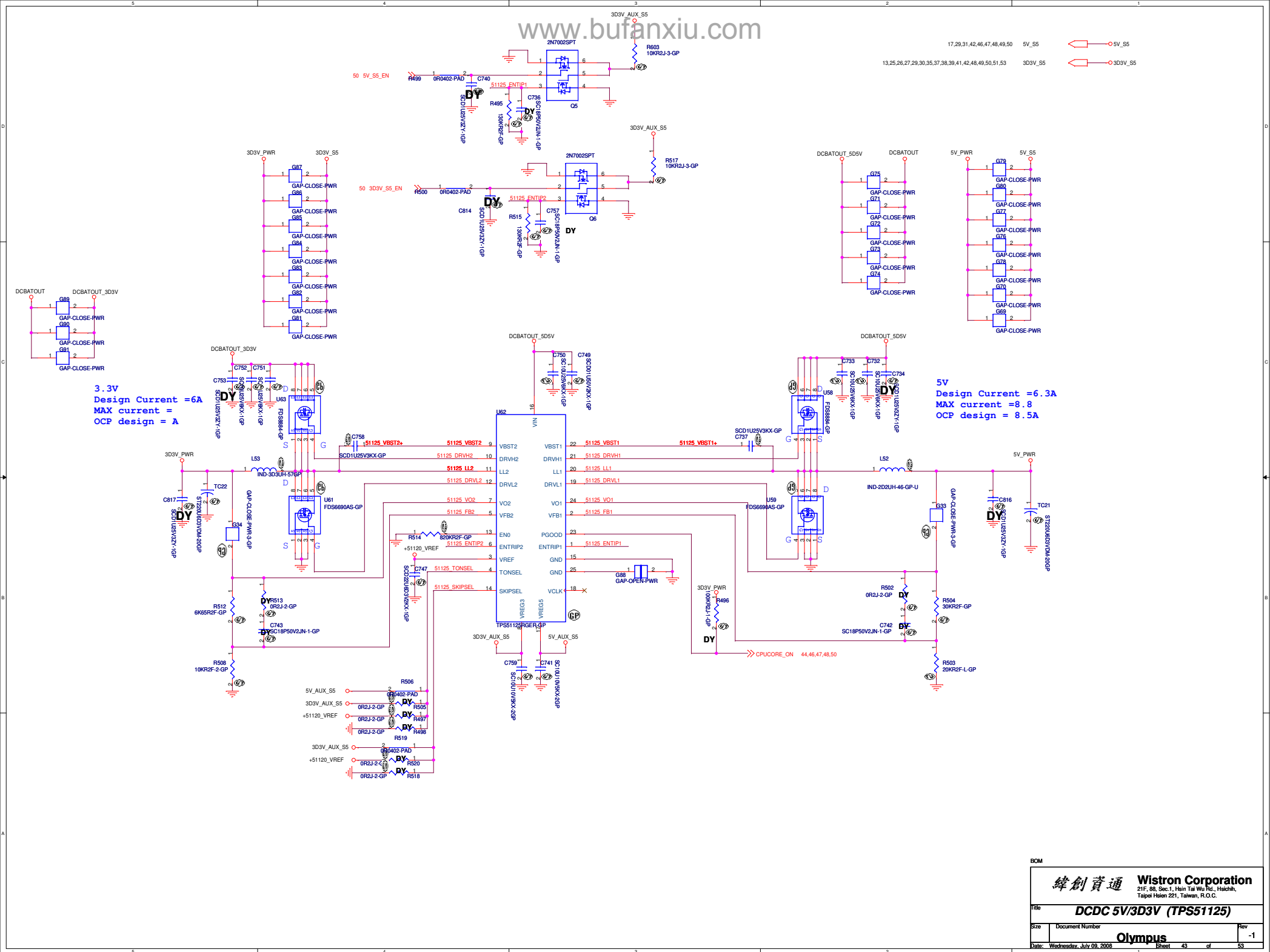


USB*2 + 1394

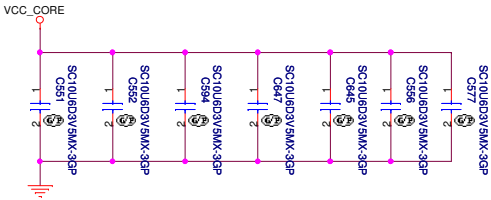


緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

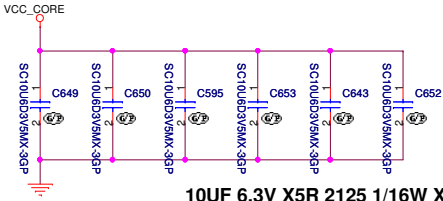
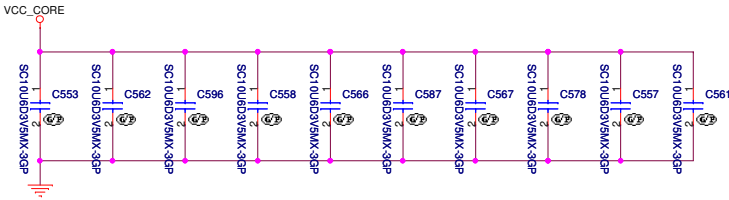
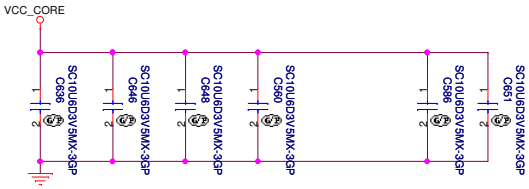
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Size B	Document Number		Rev
	Olympus		-1
Date:	Wednesday, July 09, 2008	Sheet 42 of	53





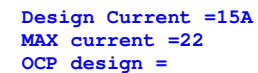


10UF 6.3V X5R 2125 1/16W X16 PCS



10UF 6.3V X5R 2125 1/16W X16 PCS

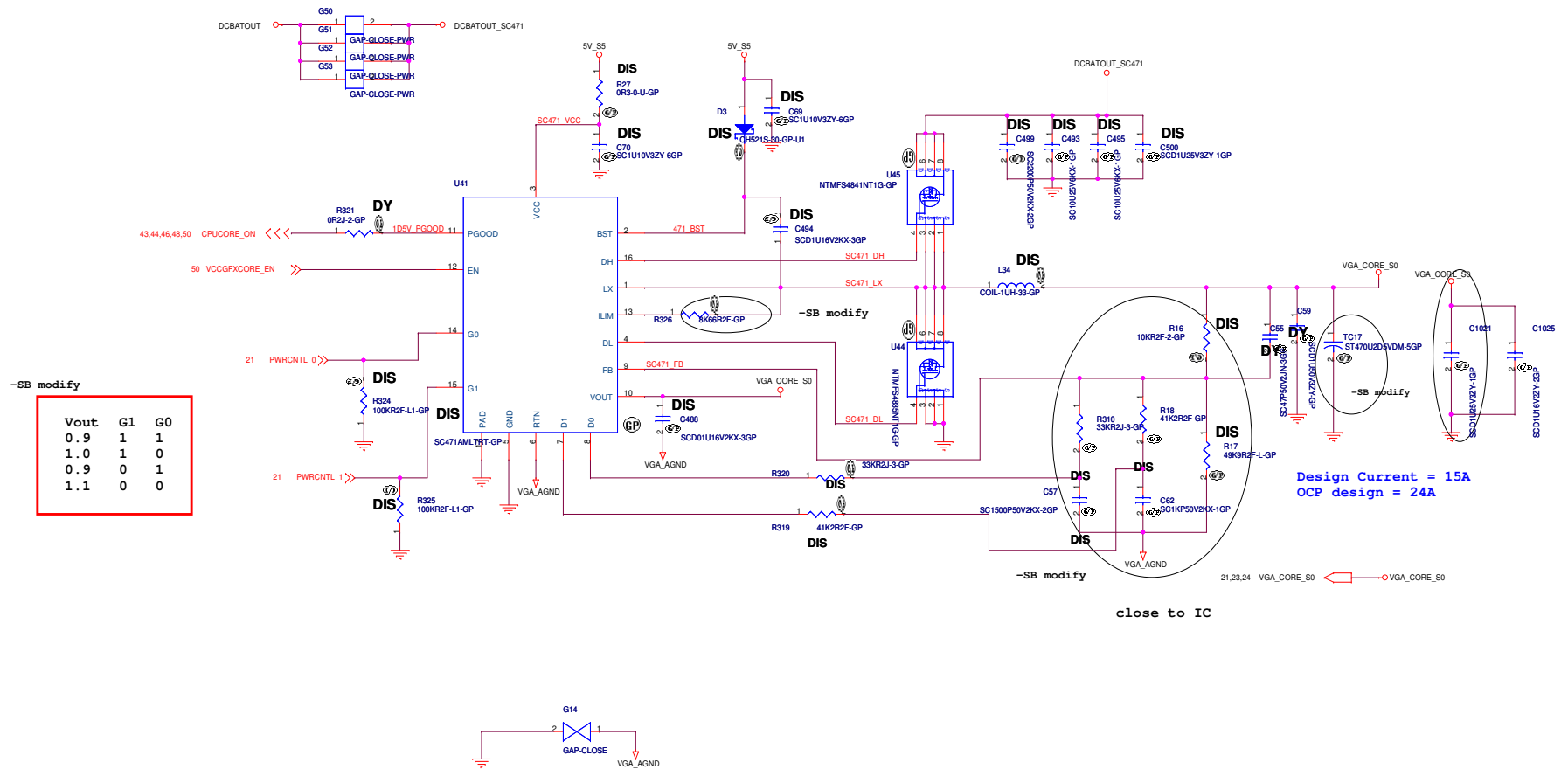
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VCCCPUCORE DECOUPLING			
Size Custom	Document Number LT32M		Rev -1
Date: Wednesday, June 18, 2008		Sheet 45 of	53



緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

SC412A +1.05VM

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LT32M	-1
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BOM

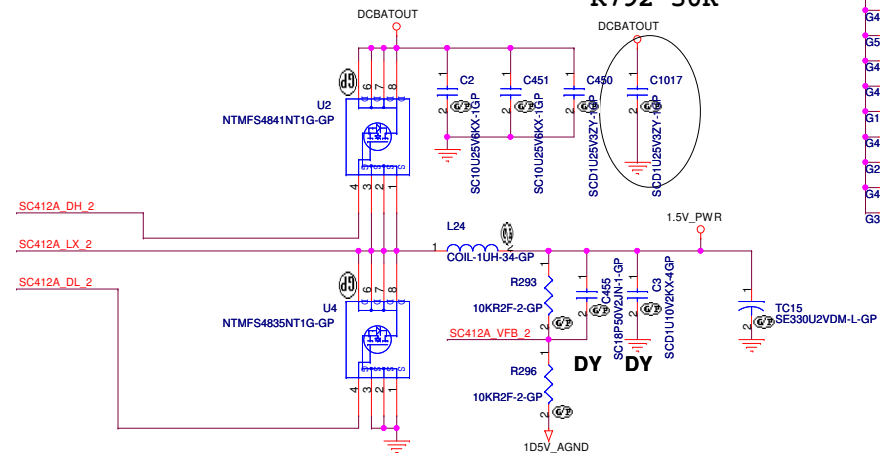
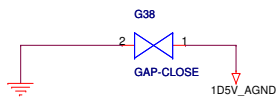
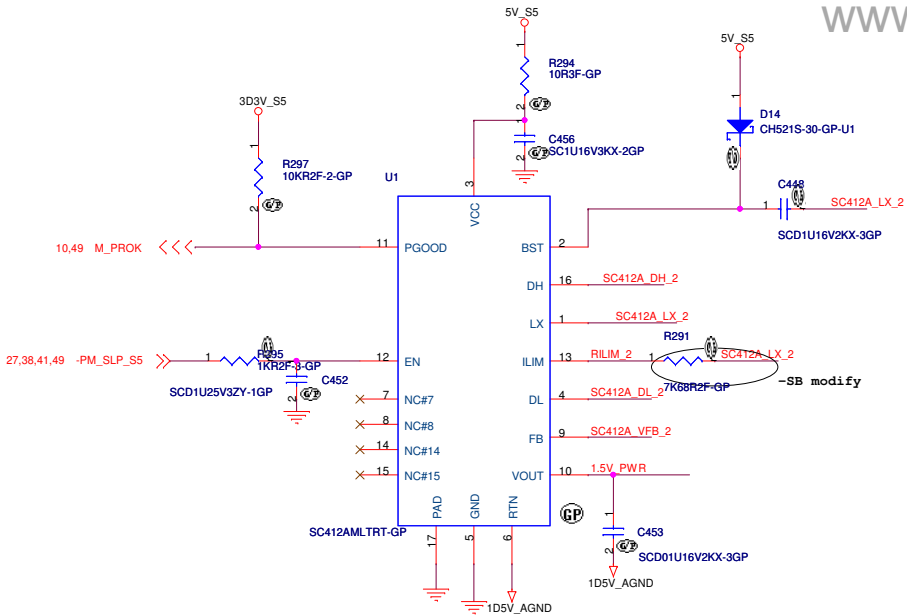
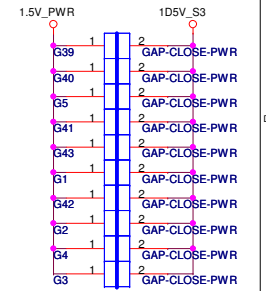
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	
SC471A VGA CORE	
Size	Document Number

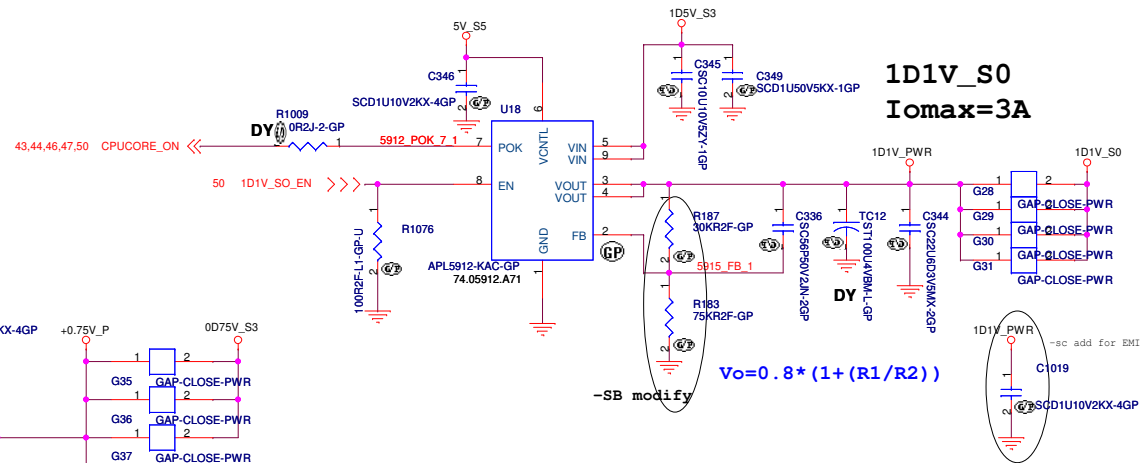
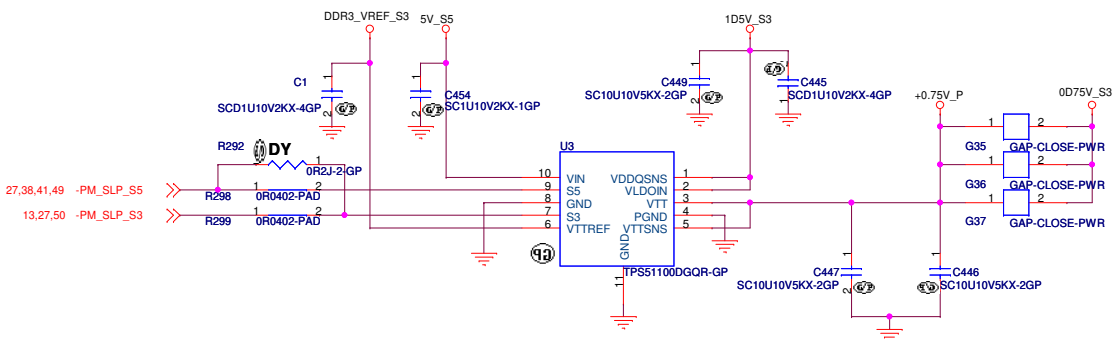
Size C	Document Number LT32M	Rev -1
Date: Wednesday, July 09, 2008		Sheet 47 of 53

Date: Wednesday, July 09, 2008 Sheet 47 of 53

```
DIS:  R791 10K
      R792 10K
UMA:  R791 42.2K
      R792 30K
```



Design Current =12A
MAX current =
OCP design =



BOM

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	SC412A 1.5V/1.1V/0.75V
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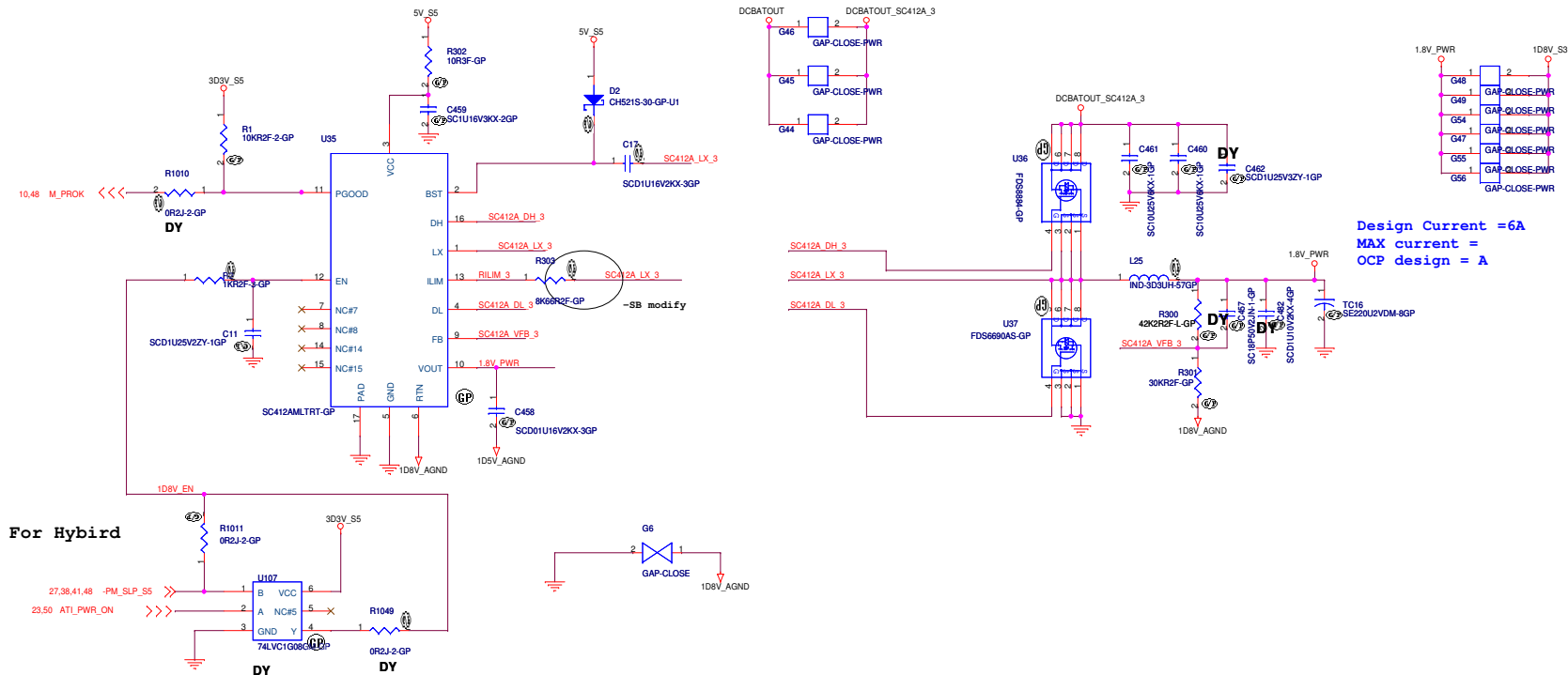
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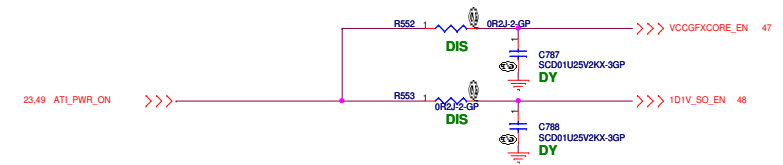
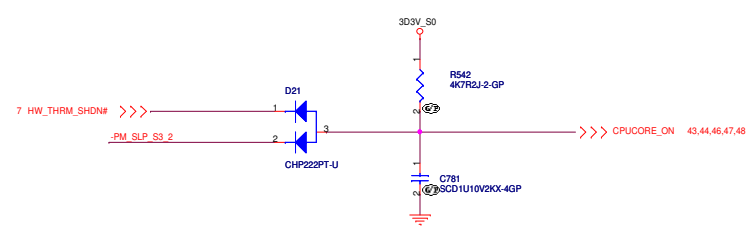
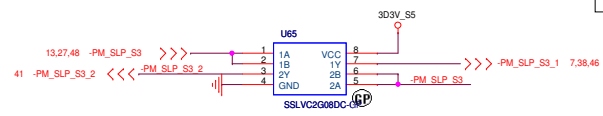
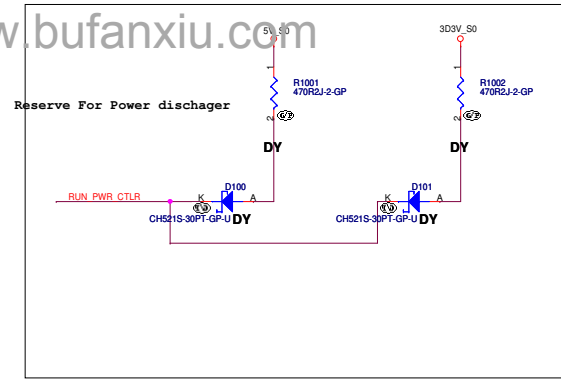
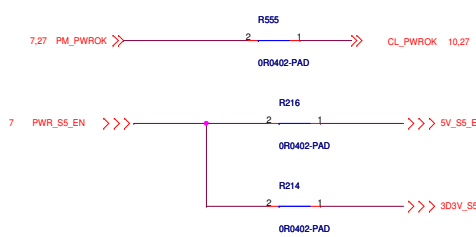
Case	Legend, Figure 3
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Olympus

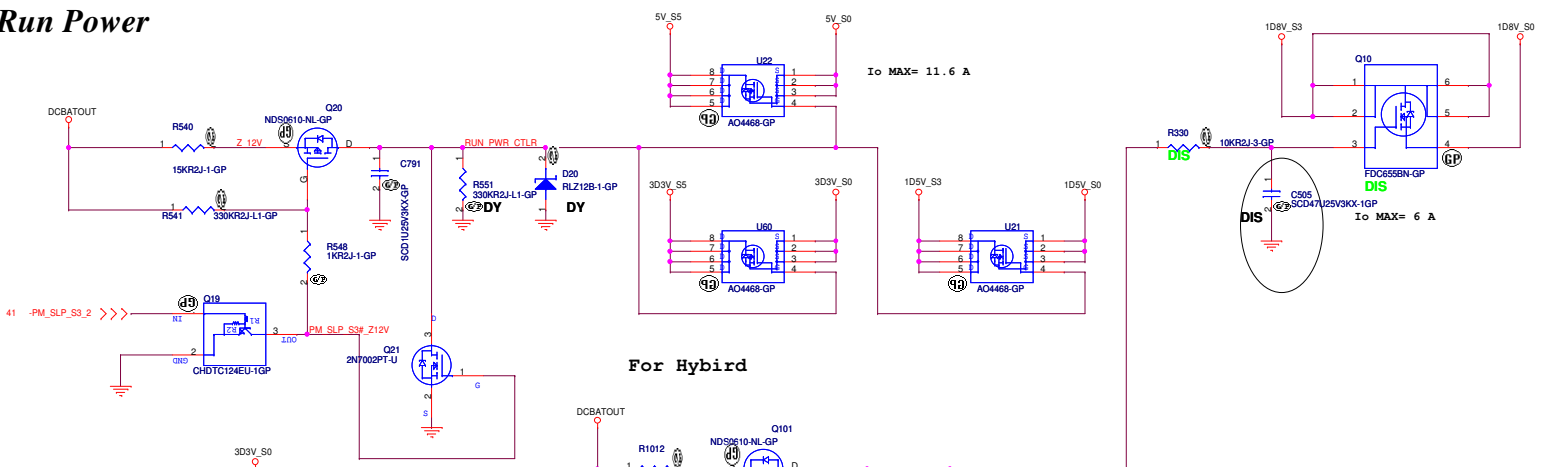
Date: Wednesday, July 09, 2008

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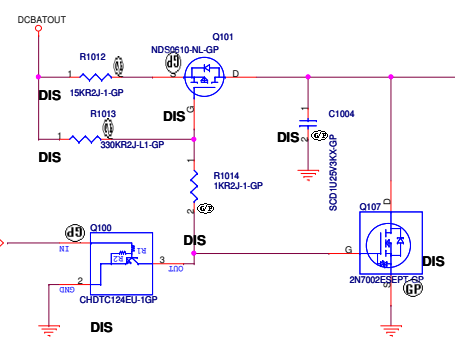
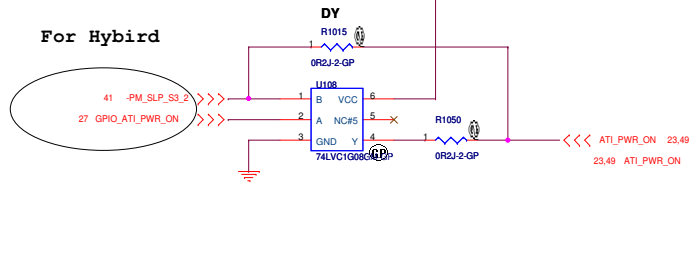


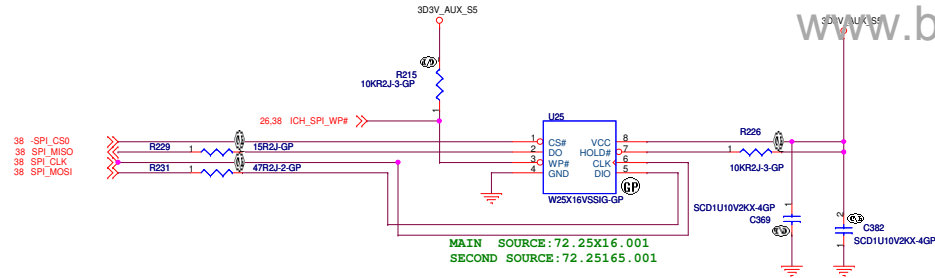
Run Power



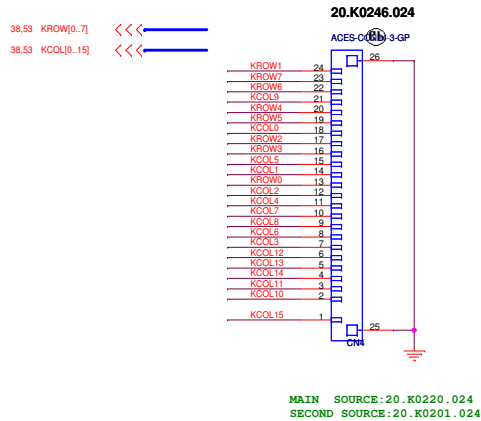
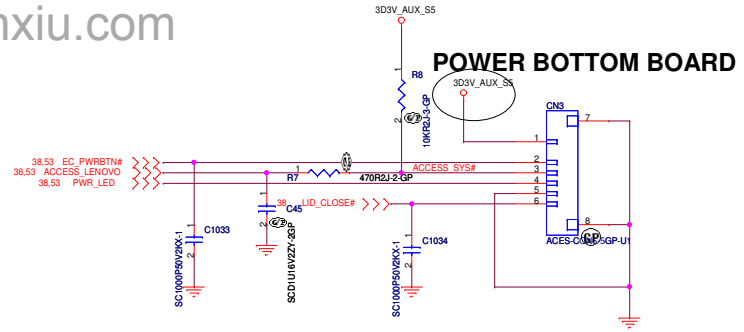
For Hybird

For Hybird

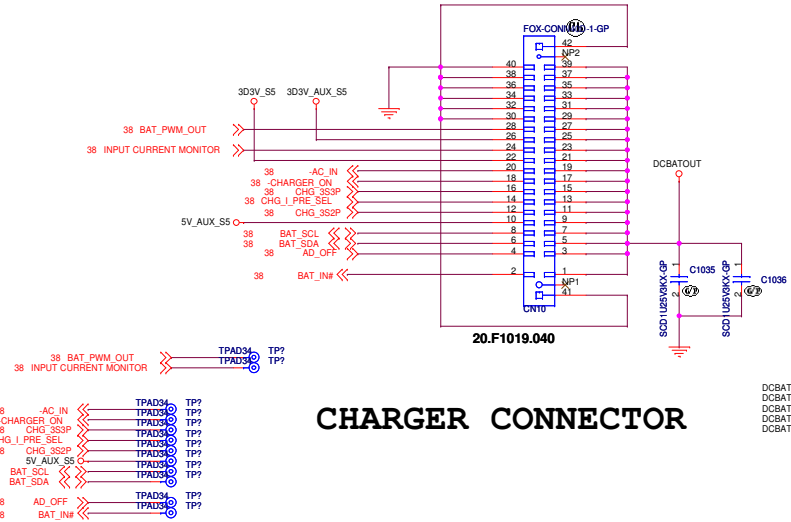




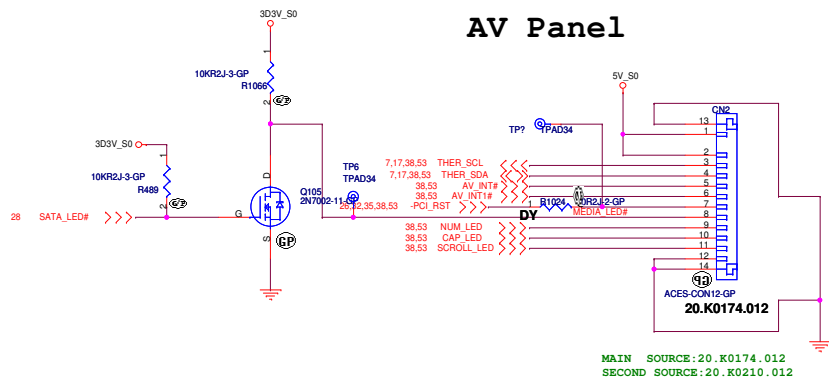
SPI FLASH



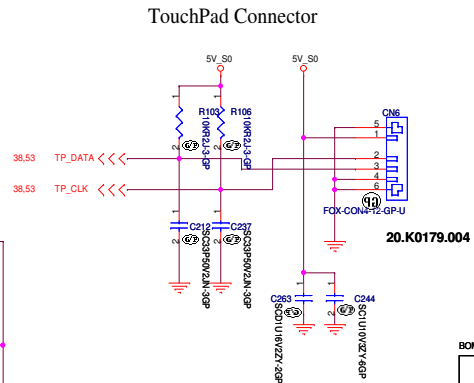
KEYBOARD CONNECTOR



CHARGER CONNECTOR

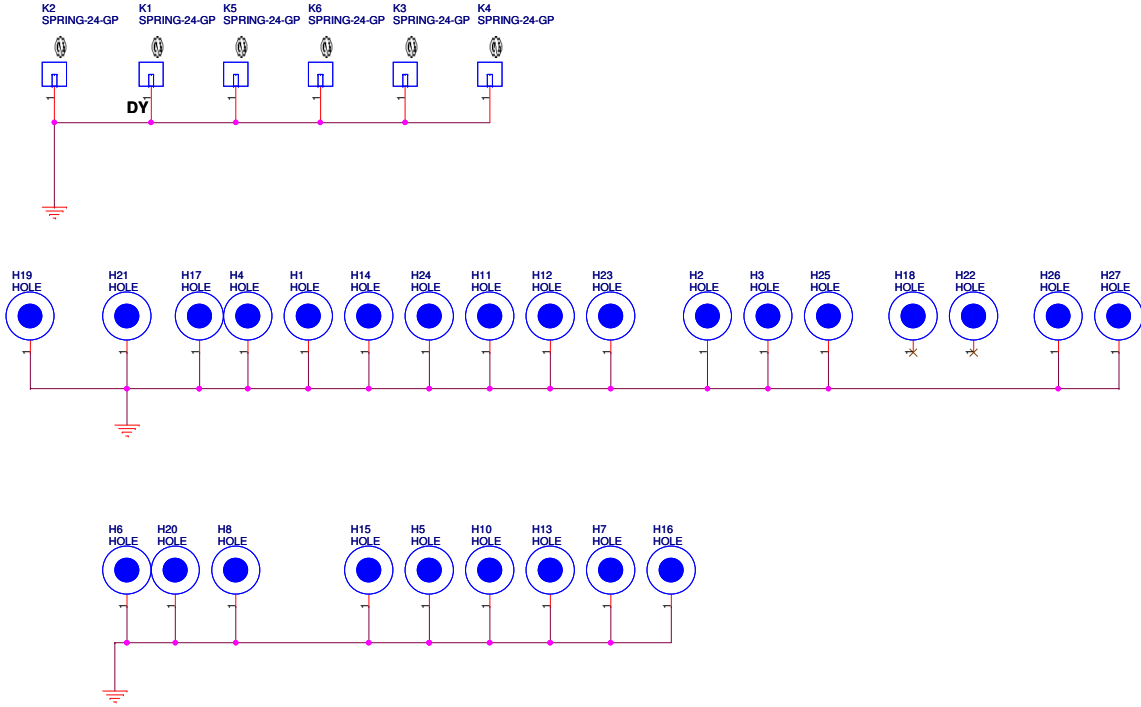


AV Panel



TouchPad Connector





BOM

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Title

PTH FOR SCREW HOLES

Size

Custom

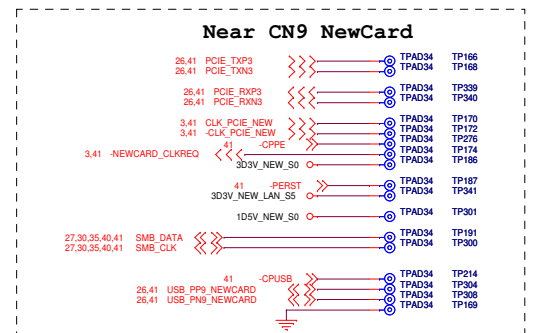
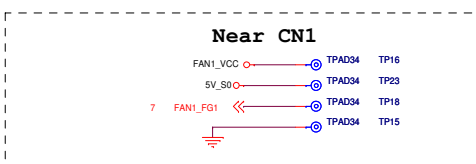
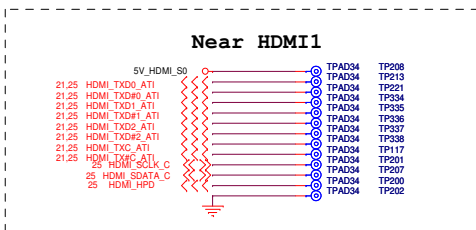
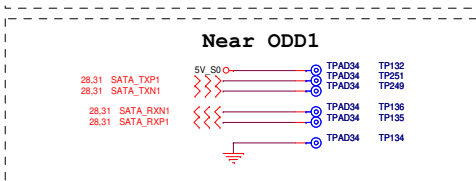
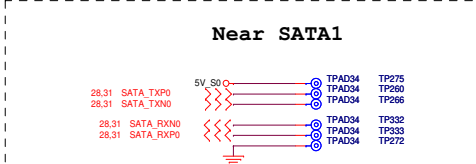
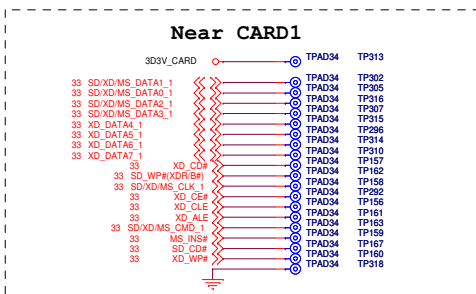
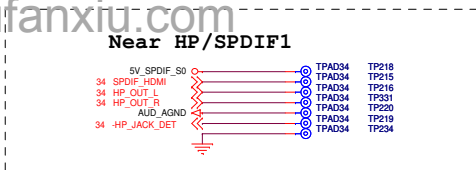
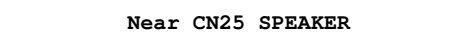
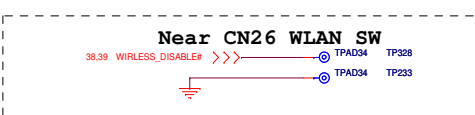
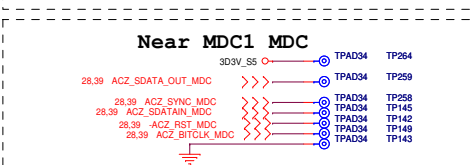
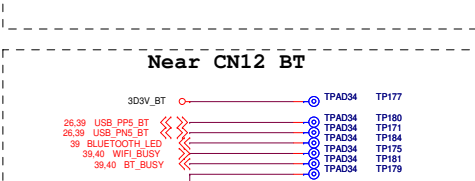
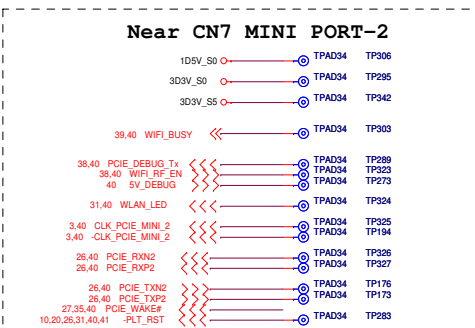
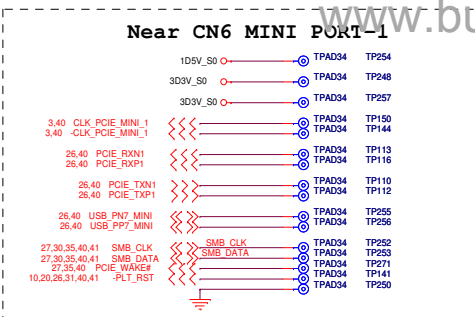
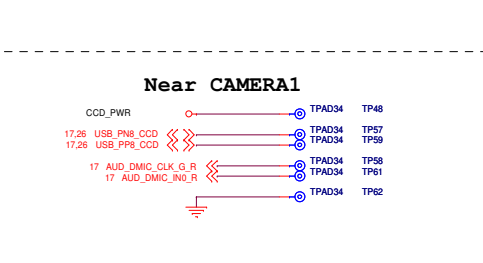
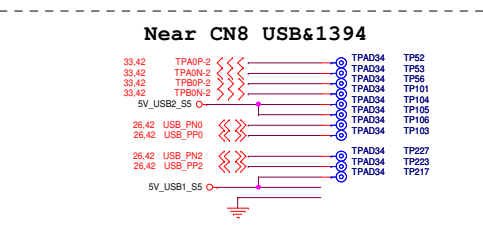
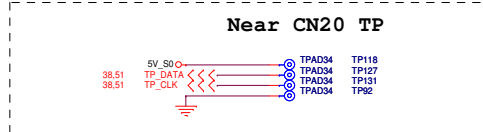
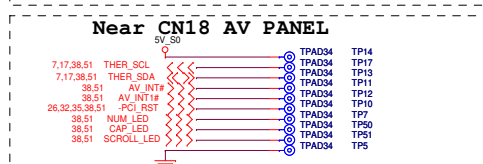
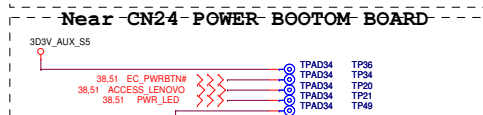
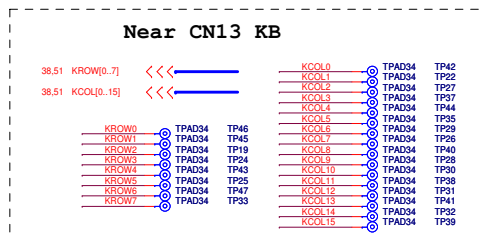
Document Number

Olympus

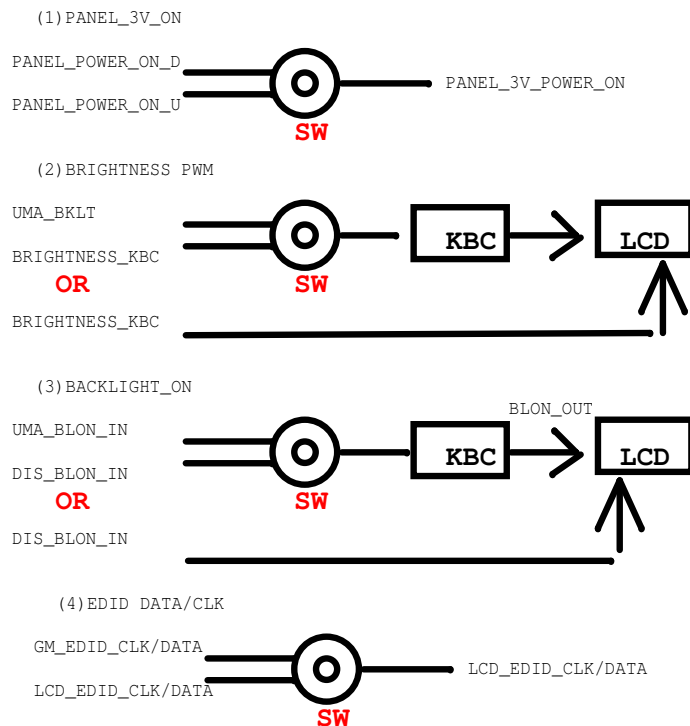
Date: Wednesday, July 09, 2008

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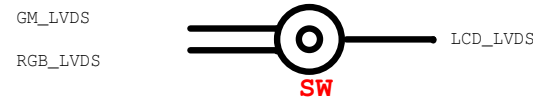
Rev -1



LCD

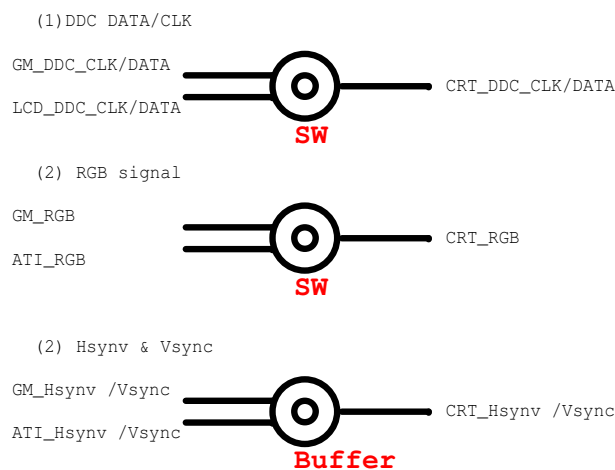


(5) LVDS signal



All the switch control by SB_GPIO52
and define
L => -UMA channel
H => -ATI channel

CRT



BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		TTEST_PAD	
Size A	Document Number		Rev -1
Date: Wednesday, June 18, 2008		Sheet 54	of 53